

PFC boost converter design guide

1200 W design example

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Application Note

About this document

Scope and purpose

This document introduces a design methodology for a Power Factor Correction (PFC) Continuous Conduction Mode (CCM) boost converter, including:

- Equations for design and power losses
- Selection guide of semiconductor devices and passive components
- Charts for CoolMOS™ optimum $R_{DS(ON)}$ selection
- 1200 W design example with calculated and experimental results.
- Schematics, layout and bill of material

Intended audience

This document is intended for design engineers who want to design CCM PFC boost converter.

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1 Introduction

Power Factor Correction (PFC) shapes the input current of the power supply to be in synchronization with the mains voltage, in order to maximize the real power drawn from the mains. In a perfect PFC circuit, the input current follows the input voltage as a pure resistor, without any input current harmonics. This document is to introduce a design methodology for the CCM PFC Boost converter, including equations for power losses estimation, selection guide of semiconductor devices and passive components, and a design example with experimental results.

1.1 Boost topology

Although active PFC can be achieved by several topologies, the boost converter (Figure 1) is the most popular topology used in PFC applications, for the following reasons:

- The line voltage varies from zero to some peak value typically 375 V; hence a step up converter is needed to output a DC bus voltage of 380 V or more. For that reason the buck converter is eliminated, and the buck-boost converter has high switch voltage stress ($V_{in}+V_o$), therefore it is also not the popular one.
- The boost converter has the filter inductor on the input side, which provides a smooth continuous input current waveform as opposed to the discontinuous input current of the buck or buck-boost topology. The continuous input current is much easier to filter, which is a major advantage of this design because any additional filtering needed on the converter input will increase the cost and reduces the power factor due to capacitive loading of the line.

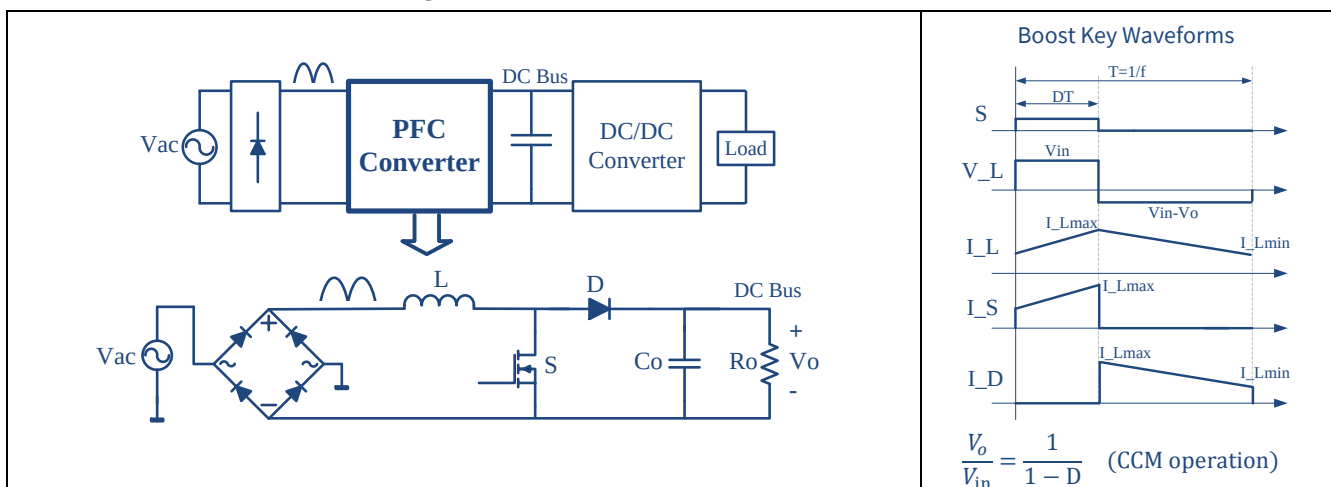


Figure 1 Structure and key waveforms of a boost converter

1.2 PFC modes of operation

The boost converter can operate in three modes: continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CrCM). Figure 2 shows modeled waveforms to illustrate the inductor and input currents in the three operating modes, for the same exact voltage and power conditions.

By comparing DCM among the others, DCM operation seems simpler than CrCM, since it may operate in constant frequency operation; however DCM has the disadvantage that it has the highest peak current compared to CrCM and also to CCM, without any performance advantage compared to CrCM. For that reason, CrCM is a more common practice design than DCM, therefore, this document will exclude the DCM design.

CrCM may be considered a special case of CCM, where the operation is controlled to stay at the boundary between CCM and DCM. CrCM usually uses constant on-time control; the line voltage is changing across the 60 Hz line cycle, the reset time for the boost inductor is varying, and the operating frequency will change as well in order to maintain the boundary mode operation. CrCM dictates the controller to sense the inductor current zero crossing in order to trigger the start of the next switching cycle.

The inductor current ripple (or the peak current) in CrCM is twice of the average value, which greatly increases the MOSFET RMS currents and turn-off current. But since every switching cycle starts at zero current, and usually with ZVS operation, turn-on loss of MOSFET is usually eliminated. Also, since the boost rectifier diode turns off at zero current as well, reverse recovery losses and noise in the boost diode are eliminated too, another major advantage of CrCM mode. Still, on the balance, the high input ripple current and its impact on the input EMI filter tends to eliminate CrCM mode for high power designs unless interleaved stages are used to reduce the input HF current ripple. A high efficiency design can be realized that way, but at substantially higher cost. That discussion is beyond the scope of this application note.

The power stage equations and transfer functions for CrCM are the same as CCM. The main differences relate to the current ripple profile and switching frequency, which affects RMS current and switching power losses and filter design.

CCM operation requires a larger filter inductor compared to CrCM. While the main design concerns for a CrCM inductor are low HF core loss, low HF winding loss, and the stable value over the operating range (the inductor is essentially part of the timing circuit), the CCM mode inductor takes a different approach. For the CCM PFC, the full load inductor current ripple is typically designed to be 20-40% of the average input current. This has several advantages:

- Peak current is lower, and the RMS current factor with a trapezoidal waveform is reduced compared to a triangular waveform, reducing device conduction losses.
- Turn-off losses are lower due to switch off at much lower maximum current.
- The HF ripple current to be smoothed by the EMI filter is much lower in amplitude.

On the other side, CCM encounters the turn-on losses in the MOSFET, which can be exacerbated by the boost rectifier reverse recovery loss due to reverse recovery charge, Q_{rr} . For this reason, ultra-fast recovery diodes or silicon carbide Schottky Diodes with extreme low Q_{rr} are needed for CCM mode.

In conclusion, we can say that for low power applications, the CrCM boost has the advantages in power saving and improving power density. This advantage may extend to medium power ranges, however at some medium power level the low filtering ability and the high peak current starts to become severe disadvantages. At this point the CCM boost starts being a better choice for high power applications.

Since this document is intended to support high power PFC applications, therefore a CCM PFC boost converter has been chosen in the application note with detailed design discussions and design examples for demonstration.

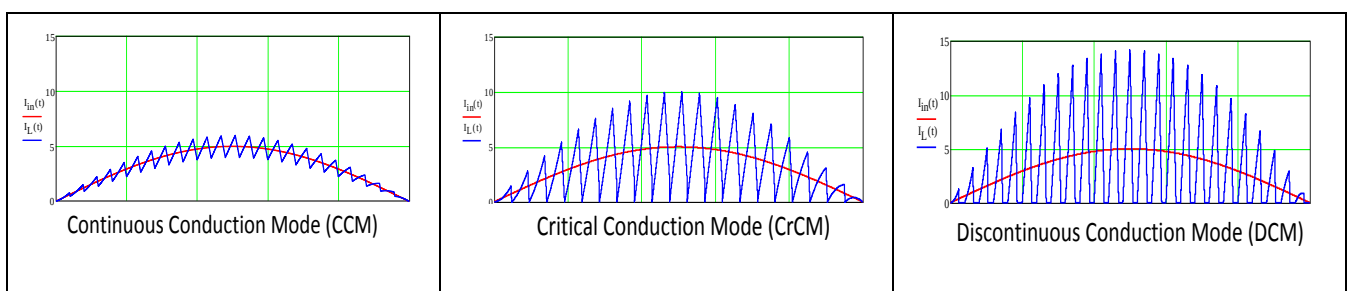


Figure 2 PFC Inductor and input line current waveforms in the three different operating modes

2 Power stage design

The following are the converter design and power losses equations for the CCM operated boost. The design example specifications listed in Table 1 will be used for all of the equations calculations. Also the boost converter encounters the maximum current stress and power losses at the minimum line voltage condition ($V_{ac.min}$); hence, all design equations and power losses will be calculated using the low-line voltage condition as an extreme case.

Table 1 Specifications of the power stage

Input voltage	85-265 V _{AC} 60 Hz
Output voltage	400 V
Maximum power steady state	1200 W
Switching frequency	100 kHz
Inductor current ripple	25% @ low line/full load
Output voltage 120Hz ripple	10 V _{p-p}
Hold-up time	16.6 ms @ V _{O,min} =340 V

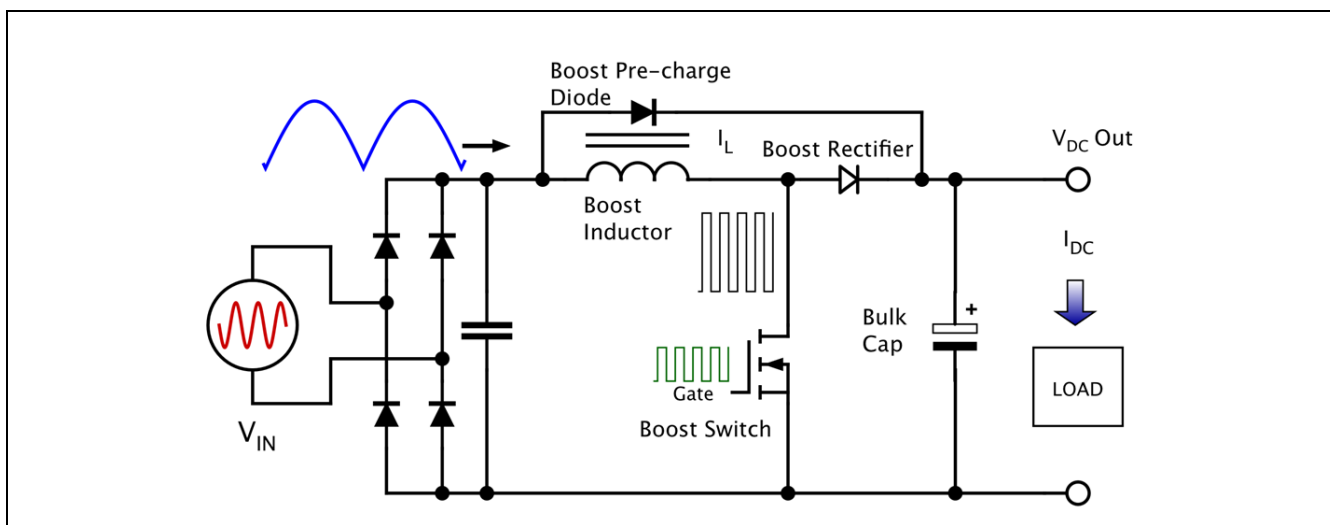


Figure 3 Block schematic for boost power stage with input rectifier

2.1 Main PFC inductor

Off-the-shelf inductors are available and usable for a first pass design, typically with single layer windings and a permeability drop of 30% or less.

In some circumstances it may be desirable to further optimize the inductor configuration in order to meet the requirements for high power factor over a wide input line current range. Many popular PFC controllers use single cycle current loop control, which can provide good performance provided that the inductor remains in CCM operation. At low-line this is no problem, but for the operation in the high-line band (176 V_{AC} to 265 V_{AC}), the operating current will be much lower. If an inductor is used with a nominal “stable” value of inductance, it works well at low-line but results in DCM mode operation for a significant part of the load range at high-line, with poorer power factor, THDi and higher EMI. A swinging choke (also called powder core), such as Arnold/Micrometals Sendust or Magnetics Inc Kool Mu, can address this if designed with the

right energy capability and with full load permeability drop by 75-80%, so that at lighter load the inductance swings up.

The filter inductor value and its maximum current are determined based on the specified maximum inductor current ripple as shown below:

$$L = \frac{1}{\%Ripple} \cdot \frac{V_{ac.min}^2}{P_o} \left(1 - \frac{\sqrt{2} \cdot V_{ac.min}}{V_o} \right) \cdot T = \frac{1}{0.25} \cdot \frac{(85 V)^2}{1200 W} \left(1 - \frac{\sqrt{2} \cdot 85 V}{400 V} \right) \cdot \frac{1}{100 \cdot 10^3 Hz} = 168.5 \mu H \quad \text{Eq. 1}$$

$$I_{L.max} = \frac{\sqrt{2} \cdot P_o}{V_{ac.min}} \cdot \left(1 + \frac{\%Ripple}{2} \right) = \frac{\sqrt{2} \cdot 1200 W}{85 V} \cdot \left(1 + \frac{0.25}{2} \right) = 22.5 A \quad \text{Eq. 2}$$

Note: Inductor saturation current must be rated at > 22.5 A.

In this evaluation board design, a 60 μ permeability Kool Mu core from Magnetics Inc. is used. It consists of two stacked of “Kool M μ ” 77083A7 toroids cores from Magnetics Inc., with 64 turns of 1.15 mm copper wire, the DC resistance is about 70 m Ω , and the inductance ranges from 680 μ H at no load dropping to about 165 μ H at low-line full load, which is very close to the desired value calculated above.



Figure 4 Main PFC inductor

Since the inductance value is varying across the line and load range, and also across the line cycle, it would be more accurate to model the inductance value as a function of V_{in} , P_o and t . in order to obtain better estimation of the switching currents and losses. This specific inductor value was modeled as shown in Figure 5.

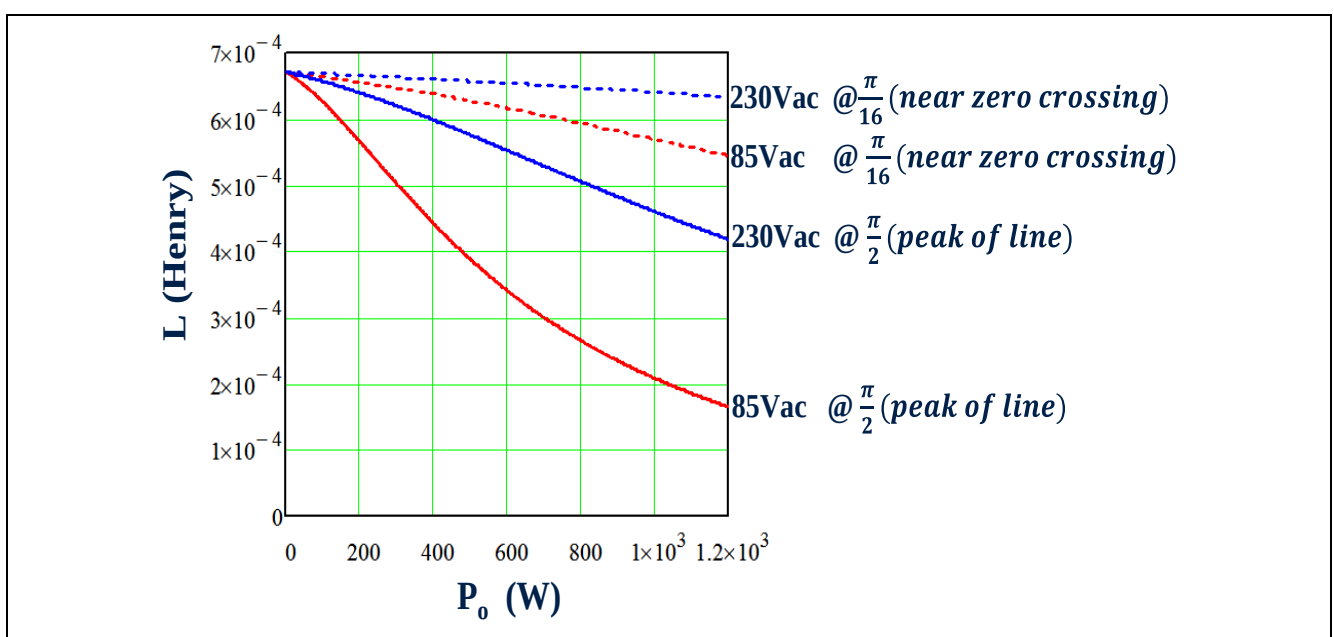


Figure 5 Swinging inductance accros load/line range

Inductor copper loss:

The inductor RMS current and the corresponding copper loss are:

$$I_{L.rms} \cong I_{in.rms} = \frac{P_o}{V_{ac.min}} = \frac{1200 \text{ W}}{85 \text{ V}} = 14.12 \text{ A} \quad \text{Eq. 3}$$

$$P_{L.cond} = I_{L.rms}^2 \cdot DCR = (14.12 \text{ A})^2 \cdot 0.07 \Omega = 13.95 \text{ W} \quad \text{Eq. 4}$$

Inductor core losses:

At low-line, core loss across the line cycle is found to be close to a sinusoidal shape (Figure 6, left). Therefore a simple and accurate enough method to estimate the average core loss is to calculate the peak core loss at the peak of the line cycle point, then multiply by $2/\pi$. However, at high line, core losses are far from the sinusoidal shape (Figure 6, right), so the aforementioned method is not valid anymore, so it is necessary to model the core loss across the line cycle as a function of time, and then integrate it to obtain the average loss.

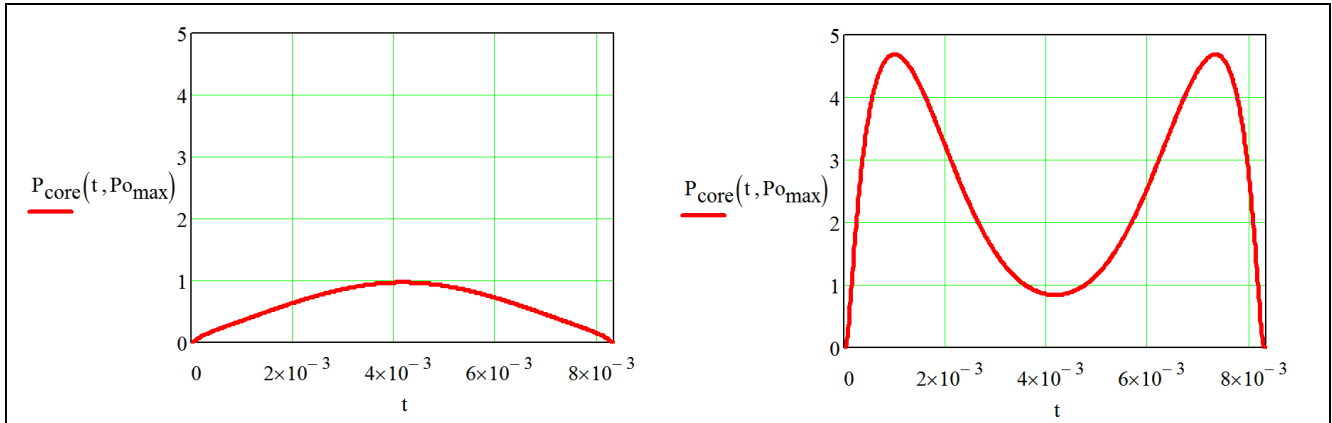


Figure 6 Inductor core loss across the line cycle: low-line (left) , high-line (right)

Since in this document we are calculating losses at the minimum line voltage, as the worst case scenario, thus we will use the first method discussed above to obtain the average core loss in the low-line, as detailed below:

In order to calculate the core loss, we must calculate the minimum and maximum inductor current and the associated minimum and maximum magnetic force (H), then we can use the fitted equation of that magnetic material to calculate the minimum and maximum magnetic flux (B). Then the AC flux swing can be used to calculate the core loss by using another fitted equation.

For 2 stacked Kool Mμ 77083A7 toroids, we get:

Path length $l_e = 98.4 \text{ mm}$ Cross section area $A_e = 2 \cdot 107 \text{ mm}^2$ Volume $V_e = 2 \cdot 10600 \text{ mm}^3$

Using the maximum inductor current calculated in Eq. 2, the magnetic force at the peak of the line cycle can be found as:

$$H_{max} = \frac{0.4 \cdot \pi \cdot N \cdot I_{L.max}}{l_e \text{ (in cm)}} = \frac{0.4 \cdot \pi \cdot 64 \text{ turns} \cdot 22.51 \text{ A}}{98.4 \text{ mm}/10} = 184 \text{ Oersteds} \quad \text{Eq. 5}$$

The minimum inductor current and magnetic force at the peak of the line cycle are:

$$I_{L.min} = \frac{P_o \cdot \sqrt{2}}{V_{ac.min}} \left(1 - \frac{\%Ripple}{2}\right) = \frac{1200 \text{ W} \cdot \sqrt{2}}{85 \text{ V}} \left(1 - \frac{25\%}{2}\right) = 17.42 \text{ A} \quad \text{Eq. 6}$$

$$H_{min} = \frac{0.4 \cdot \pi \cdot N \cdot I_{L.min}}{l_e \text{ (in cm)}} = \frac{0.4 \cdot \pi \cdot 64 \text{ turns} \cdot 17.42 \text{ A}}{98.4 \text{ mm}/10} = 142.37 \text{ Oersteds} \quad \text{Eq. 7}$$

Flux density for 60μ Koolu material is:

$$B = \left(\frac{a + b \cdot H + c \cdot H^2}{a + d \cdot H + e \cdot H^2} \right)^x \quad \text{Eq. 8}$$

where $a = 1.658e^{-2}$ $b = 1.831e^{-3}$ $c = 4.621e^{-3}$ $d = 4.7e^{-3}$ $e = 3.833e^{-5}$ $x = 0.5$

The minimum and maximum flux densities at the peak of the line cycle are:

$$B_{max} = \left(\frac{a + b \cdot H_{max} + c \cdot H_{max}^2}{a + d \cdot H_{max} + e \cdot H_{max}^2} \right)^x = 8.483 \text{ kGauss} \quad \text{Eq. 9}$$

$$B_{min} = \left(\frac{a + b \cdot H_{min} + c \cdot H_{min}^2}{a + d \cdot H_{min} + e \cdot H_{min}^2} \right)^x = 8.014 \text{ kGauss} \quad \text{Eq. 10}$$

The AC flux swing at the peak of the line cycle is:

$$\Delta B = \frac{B_{max} - B_{min}}{2} = 0.234 \text{ kGaus} \quad \text{Eq. 11}$$

Peak core loss at the peak of the line cycle is:

$$P_{core.pk} = \Delta B^2 \cdot \left(\frac{f}{10^3} \right)^{1.46} \cdot V_e \cdot 10^{-6} = 0.234^2 \cdot \left(\frac{100 \cdot 10^3}{10^3} \right)^{1.46} \cdot 2 \cdot 10600 \cdot 10^{-6} = 0.97 \text{ W} \quad \text{Eq. 12}$$

Average core loss across the line cycle is:

$$P_{core.av} = P_{core.pk} \cdot \frac{2}{\pi} = 0.968 \text{ W} \cdot \frac{2}{\pi} = 0.62 \text{ W} \quad \text{Eq. 13}$$

2.2 Rectifier bridge

Using a higher rated current bridge can reduce the forward voltage drop V_f , which reduces the total power dissipation at a small incremental cost. Also using two parallel bridges is another approach to distribute the thermal dissipation. This is often a sound strategy, as with modern components, the bridge rectifier usually has the highest semiconductor loss for the PFC stage. In this evaluation board design, 2 parallel GSIB2580 are used.

The bridge total power loss is calculated using the average input current flowing through two of the bridge rectifying diodes and is shown as:

$$I_{average} = \frac{2}{\pi} \cdot \frac{\sqrt{2} \cdot P_o}{V_{ac.min}} = \frac{2}{\pi} \cdot \frac{\sqrt{2} \cdot 1200 \text{ W}}{85 \text{ V}} = 12.71 \text{ A} \quad \text{Eq. 14}$$

$$P_{bridge} = 2 \cdot I_{average} \cdot V_{f.bridge} = 2 \cdot 12.71 \text{ A} \cdot 1 \text{ V} = 25.4 \text{ W} \quad \text{Eq. 15}$$

The selection on the heat sink is based on the process discussed in chapter 2.6 Heat sink design.

2.3 MOSFET

In order to select the optimum MOSFET, one must understand the MOSFET requirements in a CCM boost converter. High voltage MOSFETs have several families based on different technologies. For a boost converter, the following are some major MOSFET selection considerations for high efficiency application design:

- Low figure-of merits - $R_{DS(ON)} \cdot Q_g$ and $R_{DS(ON)} \cdot E_{oss}$

- Fast turn-on/off switching to reduce the device switching losses
- Gate plateau near middle of gate drive range to balance turn-on/off losses
- Low output capacitance C_{oss} for low switching energy and to increase light load efficiency
- Drain-source breakdown voltage $V_{BR(DSS)}$ to handle spikes/overshoots
- Low thermal resistance R_{thJC} . Package selection must consider the resulting total thermal resistance from junction to ambient, and the worst case surge dissipation, typically under low-line cycle skipping and recovery into highline while ramping the bulk voltage back up.
- The body diode commutation speed and reverse recovery charge are not important, since body diode never conducts in the CCM boost converter.

Several CoolMOS™ series can be used for boost applications. C7 followed by CP provides the fastest switching (Figure 7) and best performance, but require careful design in terms of gate driving circuit and PCB layout. The P6/C6/E6 series provides a cost advantage, with easier design. The P6 series approaches CP performance closely at a better price point, and is recommended for new designs that are cost sensitive. In this Evaluation board C7 is used to reach the best efficiency.

Figure 7 shows that CoolMOS™ C7 total gate charge Q_g is less than one third of the C6 charge, and less than two thirds of the CP charge. Moreover, it shows gate-drain charge Q_{gd} reduction in the much shorter length of the Miller Plateau compared to previous generations. These improvements in the gate charge profile are an indication of the improvement of the gate driving related losses as well as of the MOSFET switching times and losses.

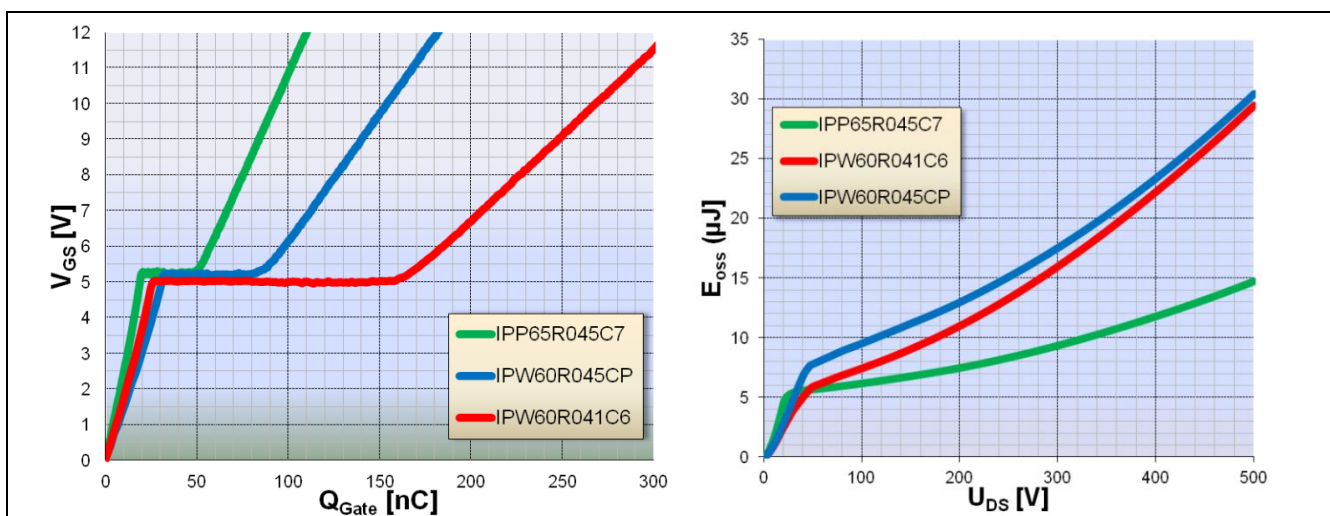


Figure 7 Gate charge and E_{oss} comparison for 41-45 mΩ CoolMOS™ C6, CP, C7

2.3.1 CoolMOS™ optimum $R_{DS(ON)}$ selection charts

Selection of the optimum on-state resistance of a specific CoolMOS™ series is based on the balancing between switching losses and conduction losses of the device at a targeted load point. This can be done by modeling all losses in software tool such as Mathcad® by evaluating different technologies and different values of the on-state resistance. This requires few iterations and entry of several parameters from the datasheet of each part.

An alternative way is using the CoolMOS™ selection charts shown in Figure 9 to Figure 12, specific charts exist for each CoolMOS™ family, optimized at half load or full load. The following is a guide on how to use these CoolMOS™ $R_{DS(ON)}$ selection charts.

Let's use the specifications in Table 1 as our design example:

$P_o = 1200$ W, $f = 100$ kHz; full load efficiency is critical; CoolMOS™ C7 is preferred for best performance.

- Step 1: Find the correct chart, Figure 8 shows the chart for CoolMOS™ C7 optimized at full load.
- Step 2: Find the 100 kHz curves (blue curves in this example)
- Step3: Mark the 1200 W on the x-axis
- Step 3: Find the 1200 W intersection with the solid blue line for the 100 kHz, read the left side y-axis, we find that 0.055 Ohm is the optimum for CoolMOS™ C7, then we may choose 045C7.
- Step 4: Find the 1200 W intersection with the dashed blue line for the 100 kHz, read the right side y-axis, we find that the 0.055 Ω will result in 13.9 W power loss at full load and low line 115 V_{AC}.

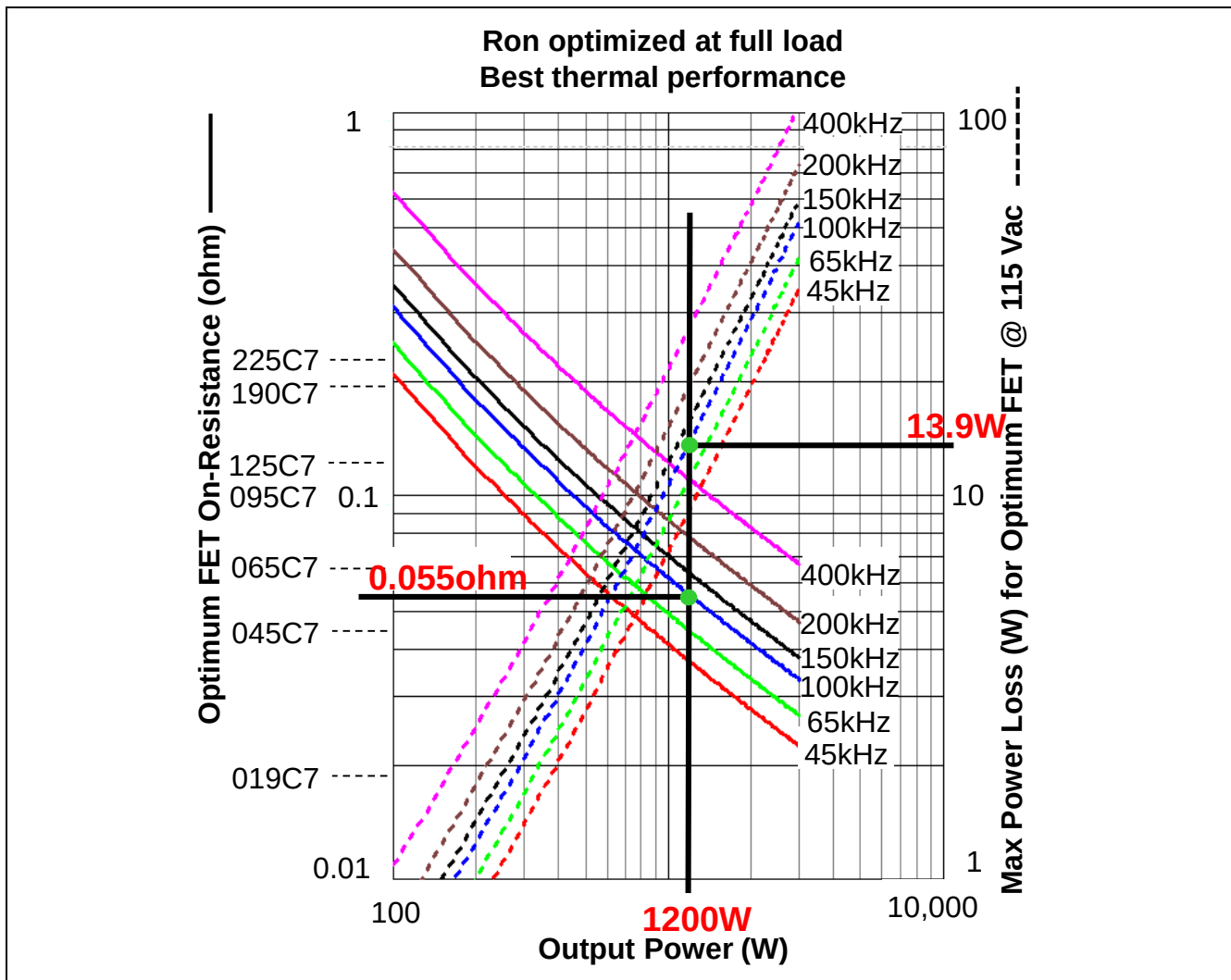
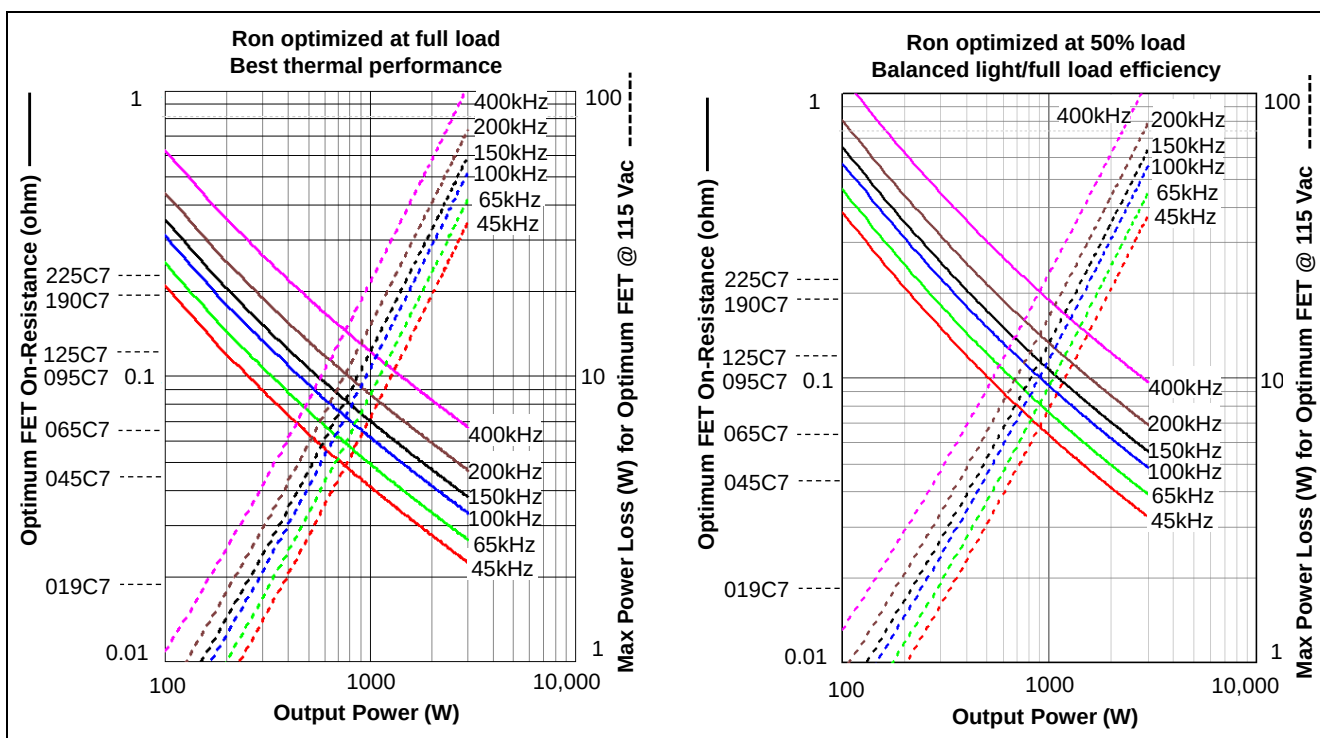
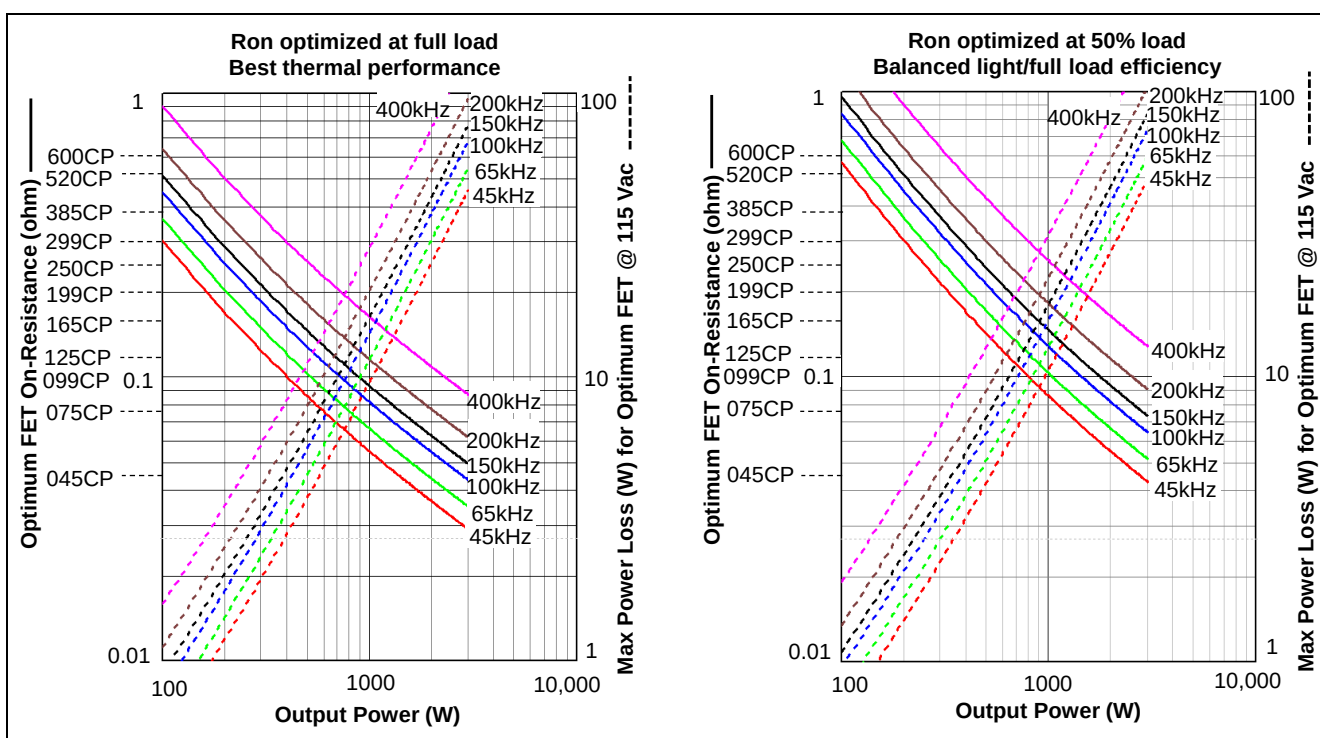
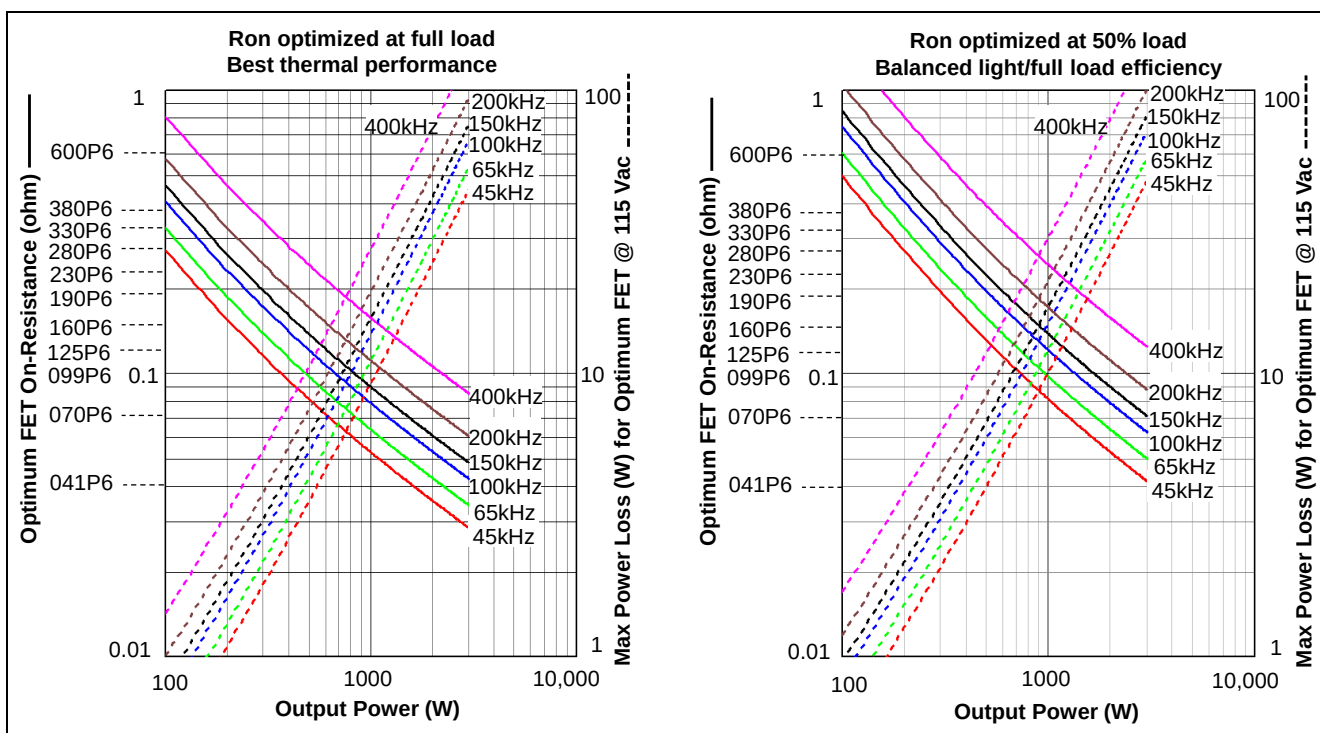
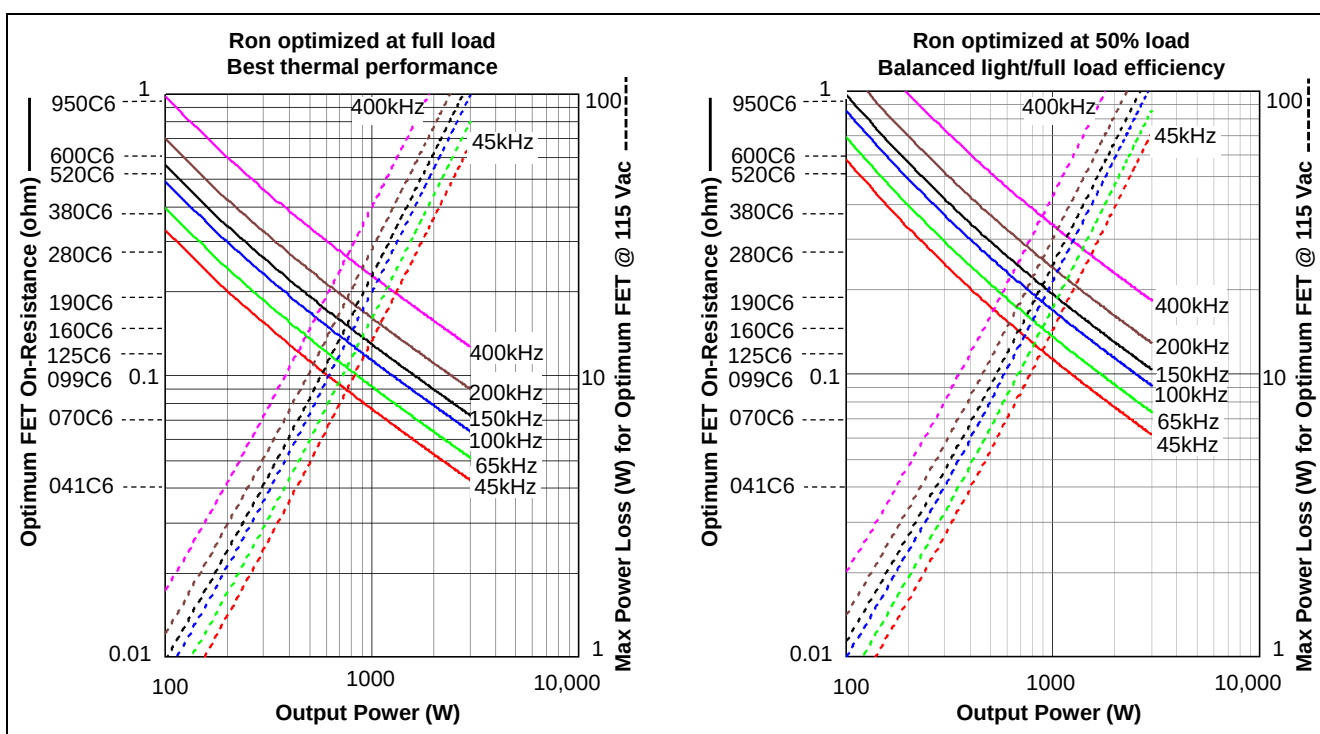


Figure 8 Example on how to use the CoolMOS™ optimum $R_{DS(on)}$ selection charts.

Figure 9 CoolMOS™ C7 optimum $R_{DS(on)}$ selection chartsFigure 10 CoolMOS™ CP optimum $R_{DS(on)}$ selection charts

Figure 11 CoolMOS™ P6 Optimum $R_{DS(on)}$ selection chartsFigure 12 CoolMOS™ C6 optimum $R_{DS(on)}$ selection charts

Since we found that 45 mΩ CoolMOS™ C7 “IPW65R045C7” is the optimum device for our design, we can base on it to calculate different power losses at the worst case of 85 Vac full load condition, as follows:

The MOSFET RMS current across the 60 Hz line cycle can be calculated by the following equation, and consequently the MOSFET conduction loss can be obtained as:

$$I_{S.rms} = \frac{P_o}{V_{ac.min}} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot V_{ac.min}}{3 \cdot \pi \cdot V_o}} = \frac{1200 \text{ W}}{85 \text{ V}} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot 85 \text{ V}}{3 \cdot \pi \cdot 400 \text{ V}}} = 12.2 \text{ A} \quad \text{Eq. 16}$$

$$P_{S.cond} = I_{S.rms}^2 \cdot R_{on(100^\circ\text{C})} = 12.2^2 \cdot (0.045 \cdot 1.8) = 12 \text{ W} \quad \text{Eq. 17}$$

(Assuming $R_{on(100^\circ\text{C})} = 1.8 \cdot R_{on(25^\circ\text{C})}$)

For switching losses calculation, the average input current is used to estimate the losses over the line cycle. The calculation is based on the switching time consideration, where the triangular area between current and voltage changing references to the switching losses.

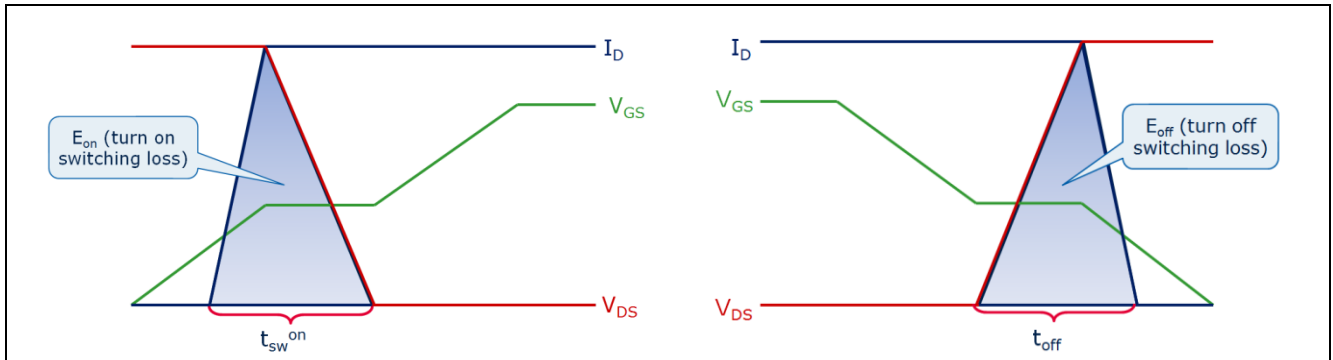


Figure 13 Simplified turn-on and turn-off waveforms

The average input current is given as:

$$I_{L.avg} = \frac{P_o}{V_{ac.min}} \cdot \frac{2 \cdot \sqrt{2}}{\pi} = \frac{1200 \text{ W}}{85 \text{ V}} \cdot \frac{2 \cdot \sqrt{2}}{\pi} = 12.71 \text{ A} \quad \text{Eq. 18}$$

Turn-on time and loss are:

$$\begin{aligned} t_{on} &= C_{iss} \cdot R_g \cdot \ln\left(\frac{V_g - V_{th}}{V_g - V_{pl}}\right) + C_{rss} \cdot R_g \cdot \left(\frac{V_{ds} - V_{pl}}{V_g - V_{pl}}\right) \\ &= 4340 \cdot 10^{-12} \text{ F} \cdot 1.8 \Omega \cdot \ln\left(\frac{12 \text{ V} - 3.5 \text{ V}}{12 \text{ V} - 5.4 \text{ V}}\right) + 75 \cdot 10^{-12} \text{ F} \cdot 1.8 \Omega \cdot \left(\frac{400 \text{ V} - 5.4 \text{ V}}{12 \text{ V} - 5.4 \text{ V}}\right) \\ &= 10 \cdot 10^{-9} \text{ s} \end{aligned} \quad \text{Eq. 19}$$

$$\left(V_{ds} = V_o = 400 \text{ V} \quad , \quad C_{rss} = \frac{Q_{gd}}{V_{ds}} = \frac{93 \cdot 10^{-9} \text{ nC}}{400 \text{ V}} = 75 \cdot 10^{-12} \text{ F} \right)$$

$$P_{S.on} = 0.5 \cdot I_{L.avg} \cdot V_o \cdot t_{on} \cdot f = 0.5 \cdot 12.71 \text{ A} \cdot 400 \text{ V} \cdot 10 \cdot 10^{-9} \text{ s} \cdot 100 \cdot 10^3 \text{ Hz} = 2.5 \text{ W} \quad \text{Eq. 20}$$

Turn-off time and loss are:

$$\begin{aligned} t_{off} &= C_{rss} \cdot R_g \cdot \left(\frac{V_{ds} - V_{pl}}{V_{pl}}\right) + C_{iss} \cdot R_g \cdot \ln\left(\frac{V_{pl}}{V_{th}}\right) \\ &= 75 \cdot 10^{-12} \text{ C} \cdot 1.8 \Omega \cdot \left(\frac{400 \text{ V} - 5.4 \text{ V}}{5.4 \text{ V}}\right) + 4340 \cdot 10^{-12} \text{ C} \cdot 1.8 \Omega \cdot \ln\left(\frac{5.4 \text{ V}}{3.5 \text{ V}}\right) = 13.3 \cdot 10^{-9} \text{ s} \end{aligned} \quad \text{Eq. 21}$$

$$P_{S.off} = 0.5 \cdot I_{L.avg} \cdot V_o \cdot t_{off} \cdot f = 0.5 \cdot 12.71 \text{ A} \cdot 400 \text{ V} \cdot 13.25 \cdot 10^{-9} \text{ s} \cdot 100 \cdot 10^3 \text{ Hz} = 3.4 \text{ W} \quad \text{Eq. 22}$$

The above is the “classic” format for calculating turn-off time and loss; due to the high Q_{oss} of Super Junction MOSFETs, the C_{oss} acts like a nonlinear capacitive snubber, and actual turn-off losses with fast switching can

be up to 50% lower than calculated. The current flow through the drain during turn-off under these conditions is non-dissipative capacitive current, and with fast drive, the channel may be completely turned off by the onset of drain voltage rise.

Output capacitance C_{oss} switching loss are:

$$P_{S,oss} = E_{oss} \cdot f = 11.7 \cdot 10^{-6} \text{ Joule} \cdot 100 \cdot 10^3 \text{ Hz} = 1.17 \text{ W} \quad \text{Eq. 23}$$

Gate drive loss is defined as:

$$P_{S,gate} = V_g \cdot Q_g \cdot f = 12 \text{ V} \cdot 93 \cdot 10^{-9} \text{ nC} \cdot 100 \cdot 10^3 \text{ Hz} = 0.11 \text{ W} \quad \text{Eq. 24}$$

Total MOSFET loss is defined as:

$$P_{S,total} = P_{S,cond} + P_{S,on} + P_{S,off} + P_{S,oss} = 19.2 \text{ W} \quad \text{Eq. 25}$$

2.3.2 TO-247 4-pin package with Kelvin source connection

In common gate drive arrangements, the fast current transient causes a voltage drop V_{LS} across the parasitic inductance of the source of the MOSFET that can counteracts the driving voltage. The induced source voltage, $V_{LS} = L \cdot di/dt$, can reduce the gate current (Figure 14), therefore lead to slowing down the switching transient and increasing the associated energy loss. On the other hand, the kelvin-source package concept is to exclude the package source inductance and layout inductance from the driving loop, so that the $L \cdot di/dt$ induced voltage is outside the gate drive loop and not affecting the gate current and switching losses. The 4pin MOSFET recommended for this design would be **IPZ65R045C7**.

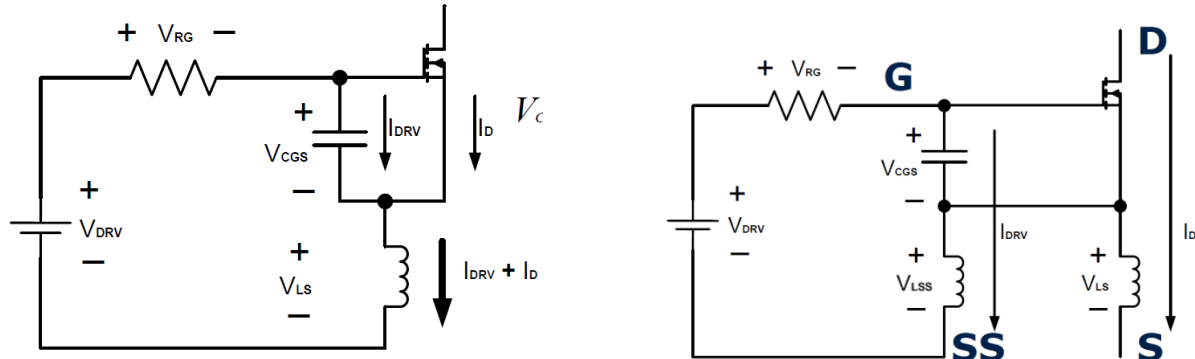


Figure 14 a) Conventional package

b) TO-247 4pin package

2.4 Boost diode

Selection of the boost diode is a major design decision in CCM boost converter. Since the diode is hard commutated at a high current, and the reverse recovery can cause significant power loss, noise and current spikes. Reverse recovery can be a bottle neck for high switching frequency and high power density power supplies. Additionally, at low line, the available diode conduction duty cycle is quite low, and the forward current quite high in proportion to the average current. For that reason, the first criteria for selecting a diode in CCM boost are fast recovery with low reverse recovery charge, followed by V_f operating at high forward current.

Since Silicon Carbide (SiC) Schottky Diodes have capacitive charge, Q_c , rather than reverse recovery charge, Q_{rr} . Their switching loss and recovery time are much lower compared to silicon ultrafast diode, and will show an enhanced performance. Moreover, SiC diodes allow higher switching frequency designs, hence, higher power density converters is achieved.

The capacitive charge for SiC diodes are not only low, but also independent on di/dt , current level, and temperature; which is different from Si diodes that have strong dependency on these conditions, as shown in Figure 15.

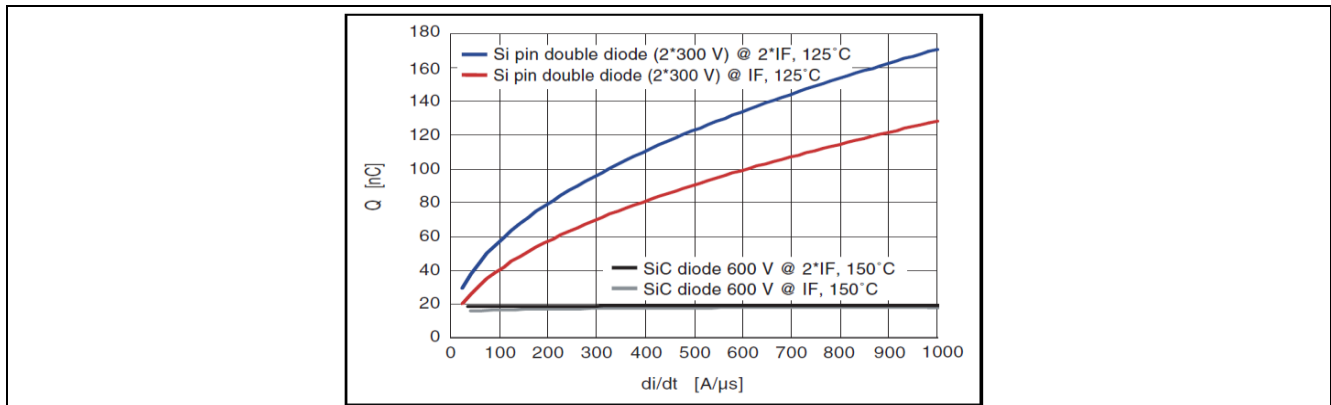


Figure 15 Capacitive charge as a function of di/dt for Si pin double diode and SiC diode

The newer generations of SiC diodes are not just Schottky devices, but are merged structure diodes known as MPS diodes - Merged PN/Schottky (Figure 16). They combine the relatively low V_f and capacitive charge characteristics of Schottky Diodes with the high peak current capability of PN diodes, while avoiding the high junction voltage penalty (typically 2.5-3 V at room temperature) of a pure PN wide bandgap diode.

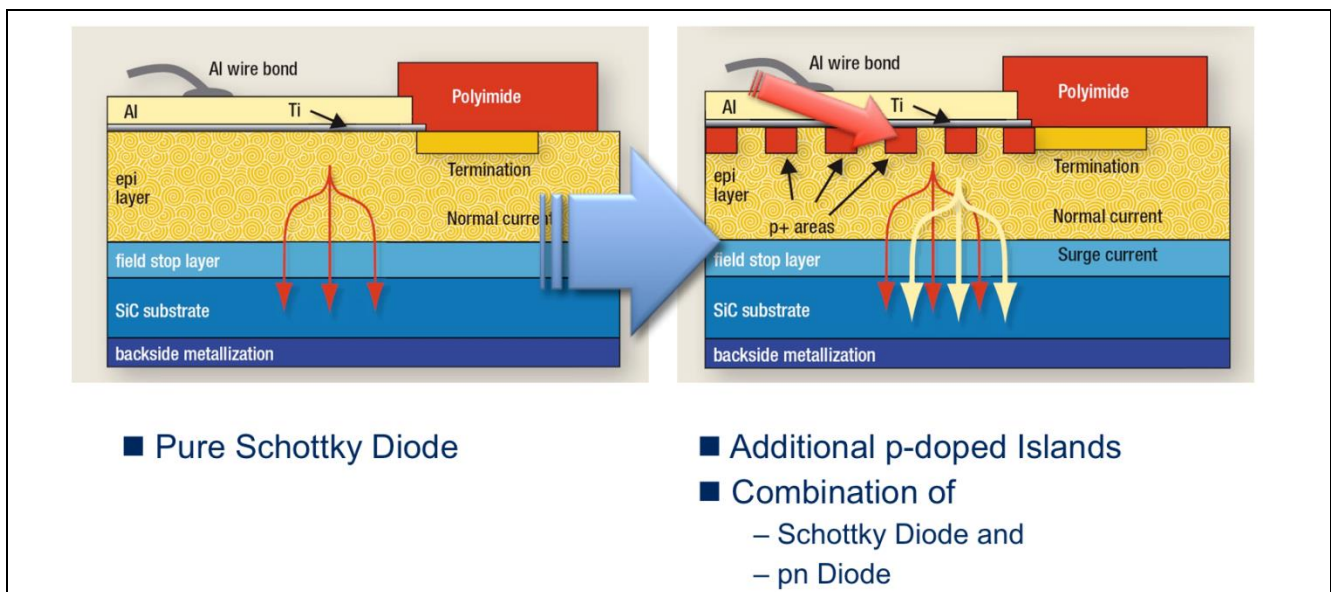


Figure 16 Schottky and Merged PN/Schottky compared

The recommended diode for CCM boost applications is the 650 V CoolSiC™ Schottky Diode Generation 5, which include Infineon's leading edge technologies, such as diffusion soldering process and wafer thinning technology. The result is a new family of products showing improved efficiency over all load conditions, coming from both the improved thermal characteristics and an improved figure-of-merit ($Q_c \times V_f$).

With the high surge current capability of the MPS diode, there is some latitude for the selection of the boost diode. A simple rule of thumb that works well for a wide input range PFC is 1 A diode rating for each 150 W of output power for good cost/performance tradeoffs, or 1 A diode rating for each 75 W for a premium performance. For example, a 600 W application will only need a 4 A rated diode, but an 8 A diode would perform better at full load. Especially at low-line operation, where the input current is quite high with a

short duty cycle, the higher rated diode will have a much lower V_f at the actual operating current, reducing the conduction losses.

Note that even when using the MPS type SiC diode, it is still preferred to use a bulk pre-charge diode as shown earlier in Figure 3. This is a low frequency standard diode with high I2t rating to support pre-charging the bulk capacitor to the peak of the AC line voltage; this is a high initial surge current stress (which should be limited by a series NTC) that is best avoided for the HF boost rectifier diode.

In this design example, we are using the 1 A/75 W rule, so for a 1200 W we require a 16 A diode, therefore SiC diode **IDH16G65C5** is selected.

The boost diode average current and conduction loss are:

$$I_{D.avg} = \frac{P_o}{V_o} = \frac{1200 \text{ W}}{400 \text{ V}} = 3 \text{ A} \quad \text{Eq. 26}$$

$$P_{D.cond} = I_{D.avg} \cdot V_{f,diode} = 3 \text{ A} \cdot 1.5 \text{ V} = 4.5 \text{ W} \quad \text{Eq. 27}$$

Diode switching loss, which is carried by the boost MOSFET is:

$$P_{D.swit} = 0.5 \cdot V_o \cdot Q_C \cdot f = 0.5 \cdot 400 \text{ V} \cdot 23 \cdot 10^{-9} \text{ nC} \cdot 100 \cdot 10^3 \text{ Hz} = 0.46 \text{ W} \quad \text{Eq. 28}$$

Diode total loss is:

$$P_{D.total} = P_{D.cond} + P_{D.swit} = 4.5 \text{ W} + 0.46 \text{ W} = 4.96 \text{ W} \quad \text{Eq. 29}$$

2.5 Output capacitor

The output capacitor is sized to meet both of the hold-up time (16.6 ms) and the low frequency voltage ripple (10 V) requirements. The capacitor value is selected to have the larger value among the two equations in below:

$$C_o \geq \frac{2 \cdot P_o \cdot t_{hold}}{V_o^2 - V_{o,min}^2} = \frac{2 \cdot 1200 \text{ W} \cdot 16.6 \cdot 10^{-3} \text{ sec}}{(400 \text{ V})^2 - (340 \text{ V})^2} = 900.9 \mu\text{F} \quad \text{Eq. 30}$$

$$C_o \geq \frac{P_o}{2 \cdot \pi \cdot f_{line} \cdot \Delta V_o \cdot V_o} = \frac{1200 \text{ W}}{2 \cdot \pi \cdot 60 \text{ Hz} \cdot 10 \text{ V} \cdot 400 \text{ V}} = 795.8 \mu\text{F} \quad \text{Eq. 31}$$

$$\rightarrow C_o = \max(900.9 \mu\text{F}, 795.8 \mu\text{F}) = 900.9 \mu\text{F}$$

In this design we use two parallel 560 μF , 450 V, with dissipation factor DF=0.2, consequently the capacitor ESR loss is obtained as below:

$$ESR = \frac{DF}{2 \cdot \pi \cdot f \cdot C_o} = \frac{0.2}{2 \cdot \pi \cdot 120 \text{ Hz} \cdot (2 \cdot 560 \mu\text{F})} = 0.237 \Omega \quad \text{Eq. 32}$$

The capacitor RMS current across the 60Hz line cycle can be calculated by the following equation.

$$I_{Co,rms} = \sqrt{\frac{8 \cdot \sqrt{2} \cdot P_o^2}{3 \cdot \pi \cdot V_{ac,min} \cdot V_o} - \frac{P_o^2}{V_o^2}} = \sqrt{\frac{8 \cdot \sqrt{2} \cdot (1200 \text{ W})^2}{3 \cdot \pi \cdot 85 \text{ V} \cdot 400 \text{ V}} - \frac{(1200 \text{ W})^2}{(400 \text{ V})^2}} = 6.47 \text{ A} \quad \text{Eq. 33}$$

$$P_{Co} = I_{Co,rms}^2 \cdot ESR = (6.47 \text{ A})^2 \cdot 0.237 \Omega = 9.91 \text{ W} \quad \text{Eq. 34}$$

2.6 Heat sink design

The MOSFET and boost diode share the same heat sink, thermal resistors are modeled as in Figure 17.

In this evaluation board the maximum heat sink temperature T_S is regulated to 60°C, so we can calculate the average junction temperature for the MOSFET and diode as follows:

$$T_{J,diode} = T_S + P_{diode} \cdot (R_{thCS,diode} + R_{thJC,diode}) \quad \text{Eq. 35}$$

$$T_{J,FET} = T_S + P_{FET} \cdot (R_{thCS,FET} + R_{thJC,FET}) \quad \text{Eq. 36}$$

The T_S can be regulated by choosing a heatsink that with certain airflow can reach the thermal resistance (R_{thSA}) calculated below:

$$R_{thSA} = \frac{T_S - T_A}{P_{FET} + P_{diode}} \quad \text{Eq. 37}$$

Where:

R_{thJC} : Thermal resistance from junction to case, this is specified in the MOSFET and Diode datasheets.

R_{thCS} : Thermal resistance from case to heatsink, typically low compared to the overall thermal resistance, its value depends on the the interface material, for example, thermal grease and thermal pad.

R_{thSA} : Thermal resistance from heatsink to ambient, this is specified in the heatsink datasheets, it depends on the heatsink size and design, and is a function of the surroundings, for example, a heat sink could have difference values for R_{thSA} for different airflow conditions.

T_S : Heatsink temperature.

T_C : Case temperature.

T_A : Ambient temperature.

P_{FET} : FET total power loss.

P_{diode} : Diode total power loss.

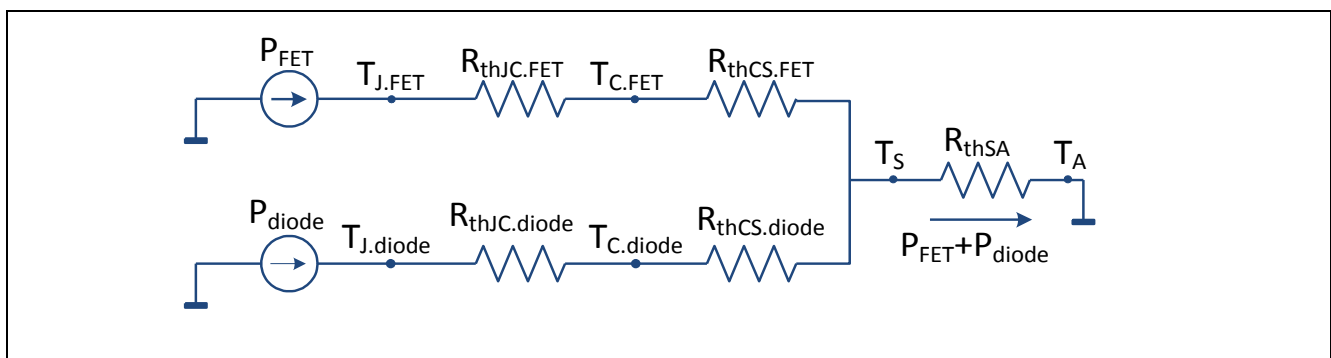


Figure 17 Schematic of thermal network

3 ICE3PCS01G PFC boost controller

The ICE3PCS01G is a 14pins controller IC for power factor correction converters. It is suitable for wide range line input applications from 85 to 265 V_{AC} and with overall efficiency above 97%. The IC supports the converters in boost topology and operates in continuous conduction mode (CCM) with average current control.

The IC operates with a cascaded control; the inner current loop and the outer voltage loop. The inner current loop of the IC controls the sinusoidal profile for the average input current. It uses the dependency of the PWM duty cycle on the line input voltage to determine the corresponding input current. This means the average input current follows the input voltage as long as the device operates in CCM. Under light load condition, depending on the choke inductance, the system may enter into discontinuous conduction mode (DCM) resulting in a higher harmonics but still meeting the Class D requirement of IEC 1000-3-2.

The outer voltage loop of the IC controls the output bulk voltage and is integrated digitally within the IC. Depending on the load condition, internal PI compensation output is converted to an appropriate DC voltage which controls the amplitude of the average input current.

The IC is equipped with various protection features to ensure safe operating for the system and the device.

3.1 Soft startup

During power up when the V_{OUT} is less than 96% of the rated level, internal voltage loop output increases from initial voltage under the soft-start control. This results in a controlled linear increase of the input current from 0 A as can be seen in Figure 17. This helps to reduce the current stress in power components.

Once V_{OUT} has reached 96% of the rated level, the soft-start control is released to achieve good regulation and dynamic response and VB_OK pin outputs 5 V indicating PFC output voltage in normal range.

3.2 Gate switching frequency

The switching frequency of the PFC converter can be set with an external resistor R_{FREQ} at pin FREQ with reference to pin SGND. The voltage at pin FREQ is typical 1V. The corresponding capacitor for the oscillator is integrated in the device and the R_{FREQ}/frequency is given in Figure 18. The recommended operating frequency range is from 21 kHz to 250 kHz. As an example, a R_{FREQ} of 43 kΩ at pin FREQ will set a switching frequency f_{sw} of 100 kHz typically.

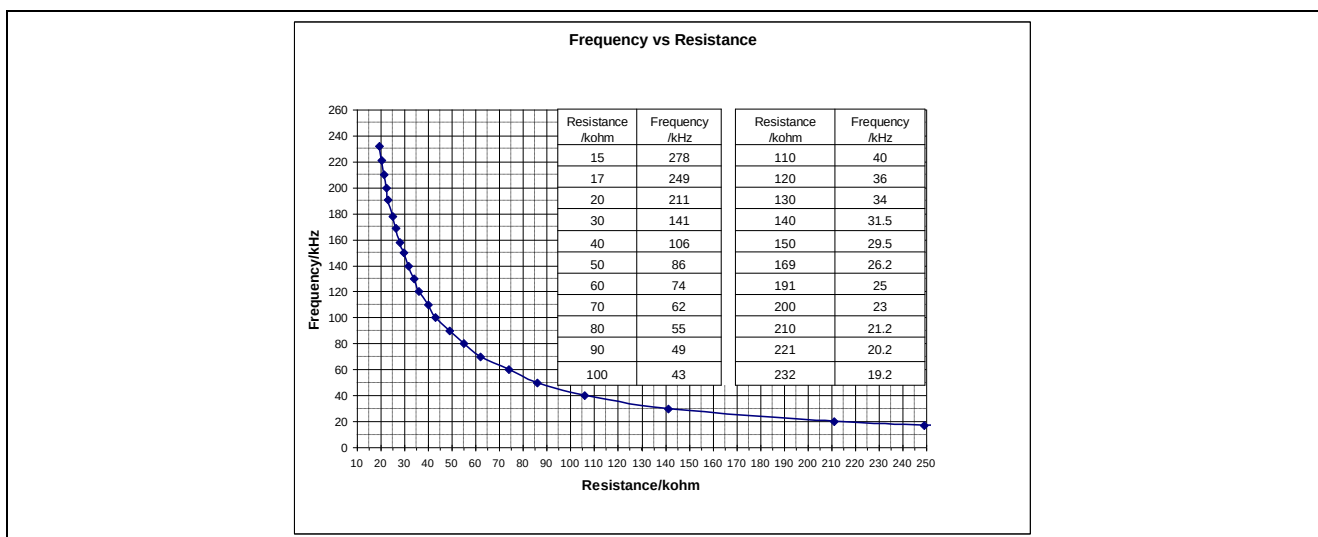


Figure 18 Frequency setting

3.3 Protection features

3.3.1 Open loop protection (OLP)

The open loop protection is available for this IC to safe-guard the output. Whenever voltage at pin V_{SENSE} falls below 0.5 V, or equivalently V_{OUT} falls below 20% of its rated value, it indicates an open loop condition (i.e. V_{SENSE} pin not connected). In this case, most of the blocks within the IC will be shutdown. It is implemented using a comparator with a threshold of 0.5 V.

3.3.2 First over-voltage protection (OVP1)

Whenever V_{OUT} exceeds the rated value by 8%, the first over-voltage protection OVP1 is active. This is implemented by sensing the voltage at pin V_{SENSE} with respect to a reference voltage of 2.7 V. A V_{SENSE} voltage higher than 2.7 V will immediately block the gate signal. After bulk voltage falls below the rated value, gate drive resumes switching again.

3.3.3 Peak current limit

The IC provides a cycle by cycle peak current limitation (PCL). It is active when the voltage at pin I_{SENSE} reaches -0.2 V. This voltage is amplified by a factor of -5 and connected to comparator with a reference voltage of 1.0 V. A deglitcher with 200 ns after the comparator improves noise immunity to the activation of this protection. In other words, the current sense resistor should be designed lower than -0.2 V PCL for normal operation.

3.3.4 IC supply under voltage lockout

When V_{CC} voltage is below the under voltage lockout threshold $V_{CC,UVLO}$, typical 11 V, IC is off and the gate drive is internally pull low to maintain the off state. The current consumption is down to 1.4 mA only.

3.3.5 Bulk voltage monitor and enable function (VBTHL_EN)

The IC monitors the bulk voltage status through V_{SENSE} pin and output a TTL signal to enable PWM IC or control inrush relay. During soft-start once the bulk voltage is higher than 95% rated value, pin VB_OK outputs a high level. The threshold to trigger the low level is decided by the pin $VBTHL$ voltage adjustable externally.

When pin $VBTHL$ is pulled down externally lower than 0.5 V most function blocks are turned off and the IC enters into standby mode for low power consumption. When the disable signal is released the IC recovers by soft-start.

4 Efficiency and power losses modeling

The design example discussed in this document was modeled in Mathcad®. All of the power losses equations were written as a function of the output power in order to be able to plot an estimated efficiency curve across the output power range as shown in Figure 19.

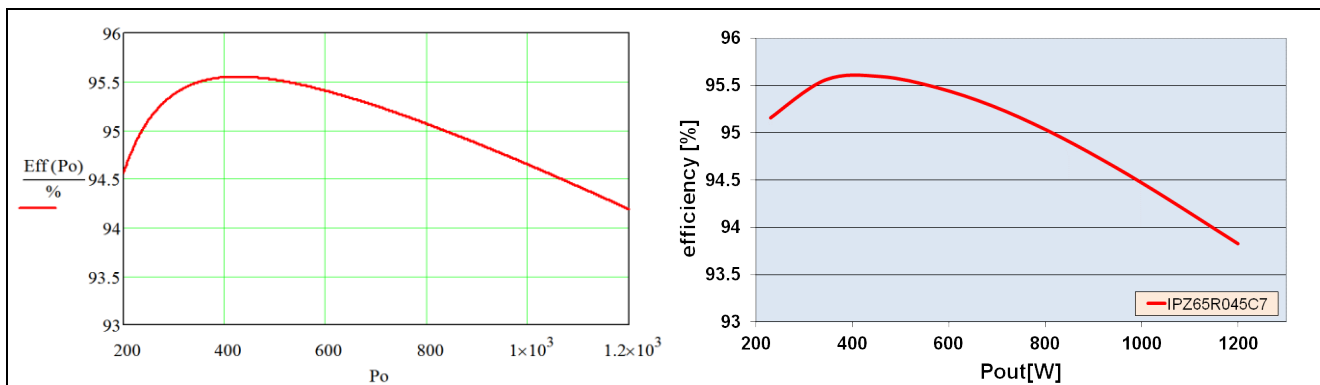


Figure 19 Calculated efficiency @ 85V_{AC} vs experimental efficiency @ 90V_{AC}

Figure 20 shows a breakdown of main power losses at the full load of both low and high line conditions.

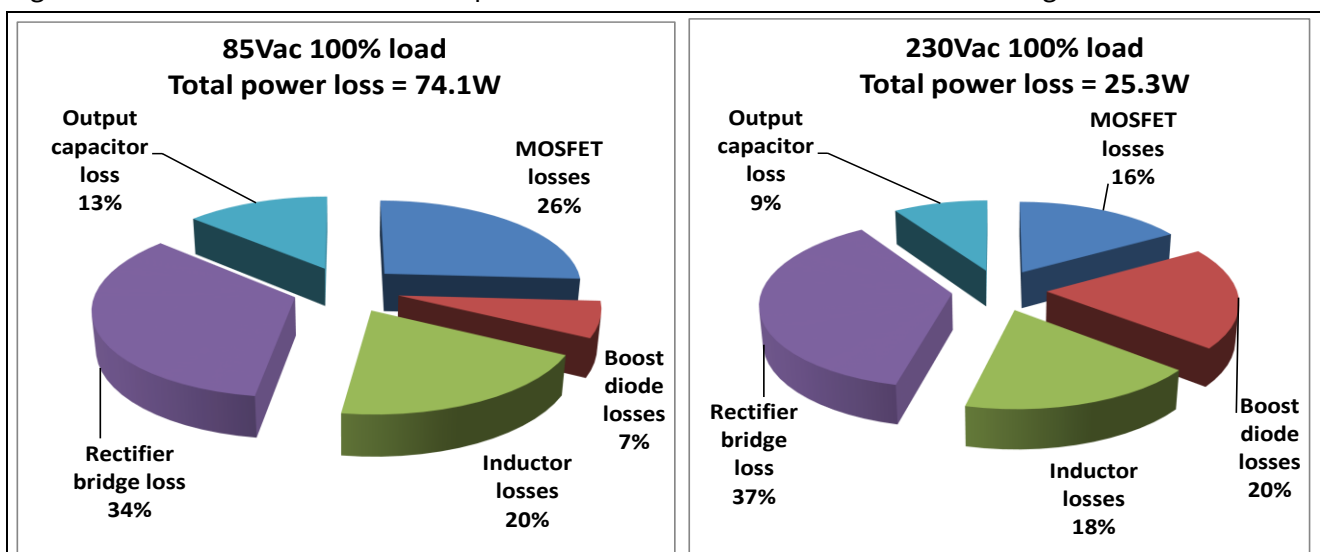


Figure 20 Breakdown of main power losses

Figure 21 shows the simulated and experimental inductor current at the low line full load condition.

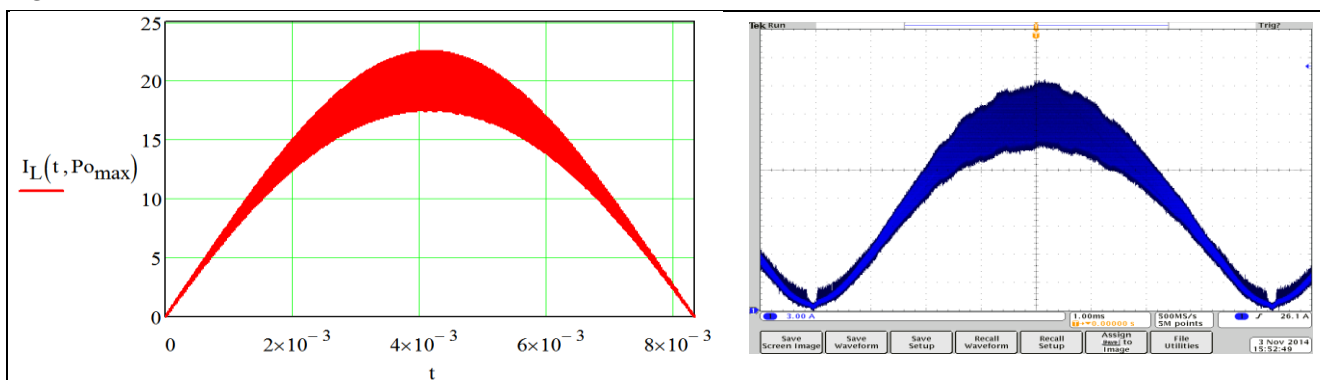


Figure 21 Simulated and experimental Inductor current waveforms at low-line full load condition

5 Experimental results

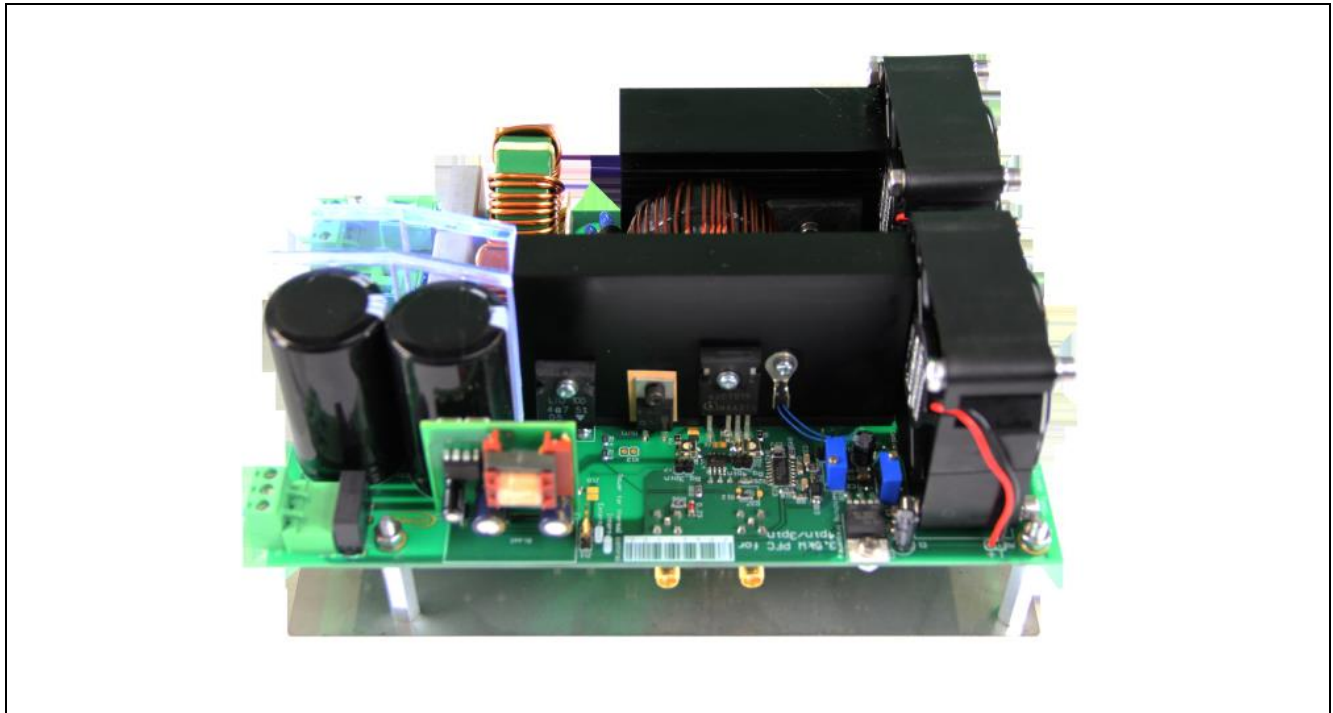


Figure 22 Evaluation board

All test conditions are based on 60°C heat sink temperature.

5.1 Load and line measurement data

The test data of the evaluation board under different test conditions are listed in Table 2. The corresponding efficiency waveforms are shown in Figure 23 and Figure 24.

Table 2 Efficiency test data with IPZ65R045C7 & IDH12G65C5 @ 100kHz, $R_g = 1.8 \Omega$

Input	V_{IN} [V]	I_{IN} [A]	P_{IN} [W]	U_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	Efficiency [%]	Power factor
90 V _{AC}	88.88	14.3962	1278.5	402.05	2.984	1200.02	93.829	0.9996
	89.11	10.8743	968.8	402.09	2.282	917.68	94.719	0.9997
	89.33	8.0877	722.4	402.12	1.711	688.38	95.290	0.9998
	89.51	5.3667	480.2	402.15	1.141	459.05	95.597	0.9996
	89.74	2.6953	241.5	402.18	0.571	229.82	95.161	0.9984
230 V _{AC}	229.5	5.3365	1222.1	402.03	2.985	1200.01	98.186	0.9976
	229.6	4.431	1014.9	402.06	2.479	996.66	98.198	0.9975
	229.7	3.3171	758.7	402.10	1.852	744.59	98.138	0.9956
	229.8	2.2298	508.8	402.12	1.239	498.18	97.910	0.9929
	229.9	1.1304	253.4	402.16	0.612	246.15	97.120	0.9752

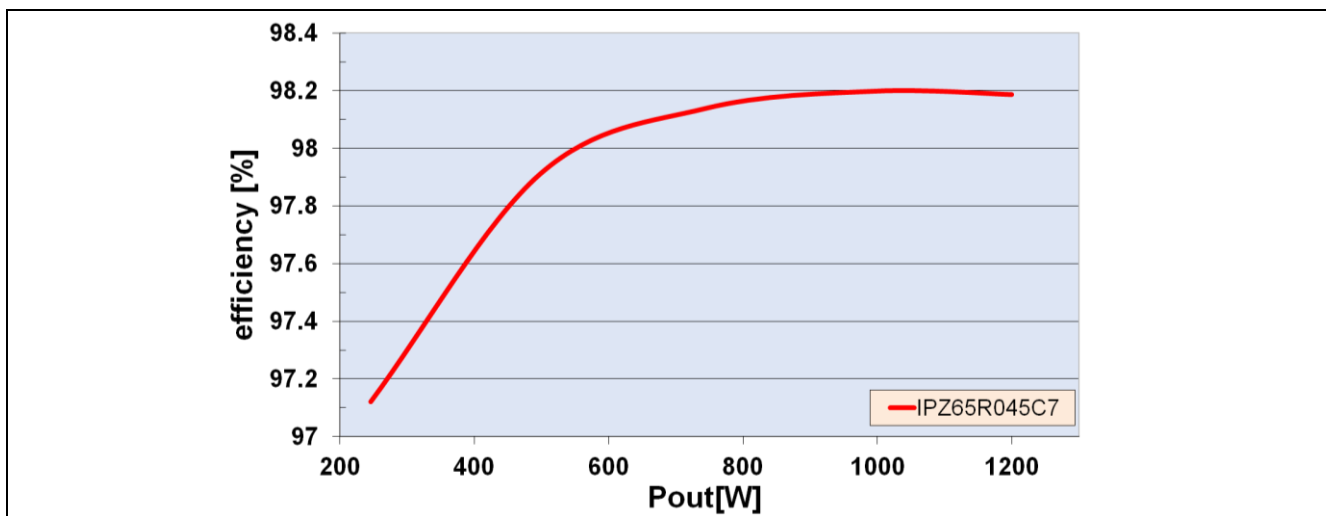


Figure 23 High-line efficiency with IPZ65R045C7 & IDH12G65C5 @ 100kHz, $R_g = 1.8 \Omega$

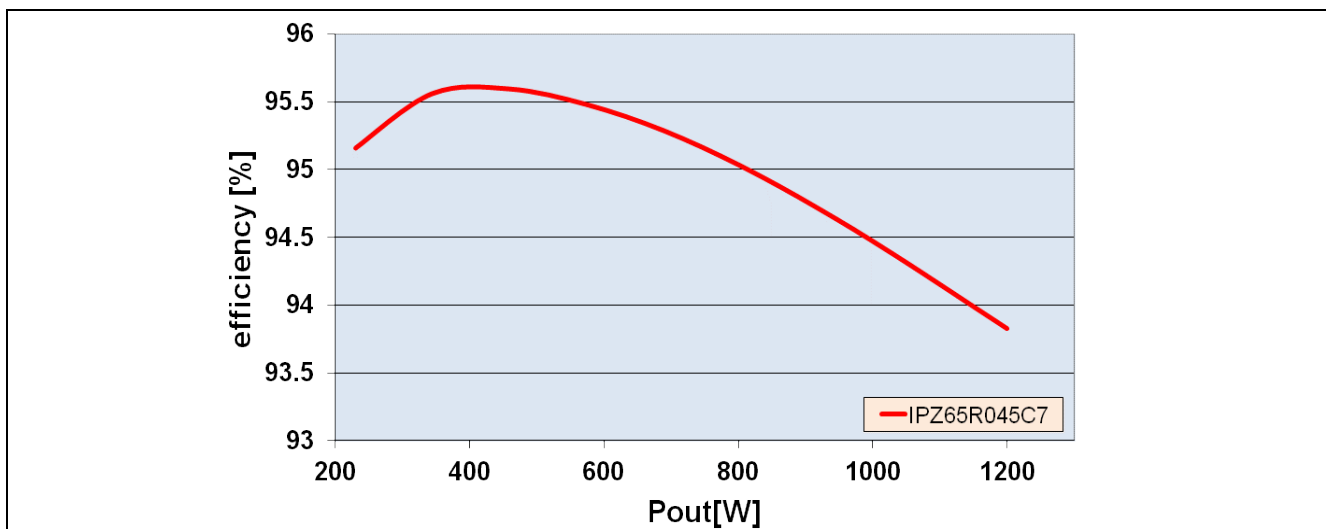


Figure 24 Low-line efficiency with IPZ65R045C7 & IDH12G65C5 @ 100kHz, $R_g = 1.8 \Omega$

5.2 Conductive EMI test

Compliance with EN55022 standard is a very important quality factor for a power supply. The EMI has to consider the whole SMPS and is split into radiated and conductive EMI consideration. For the described evaluation PFC board it is most important to investigate on the conducted EMI-behavior since it is the input stage of any SMPS below a certain power range, as shown in Figure 25.

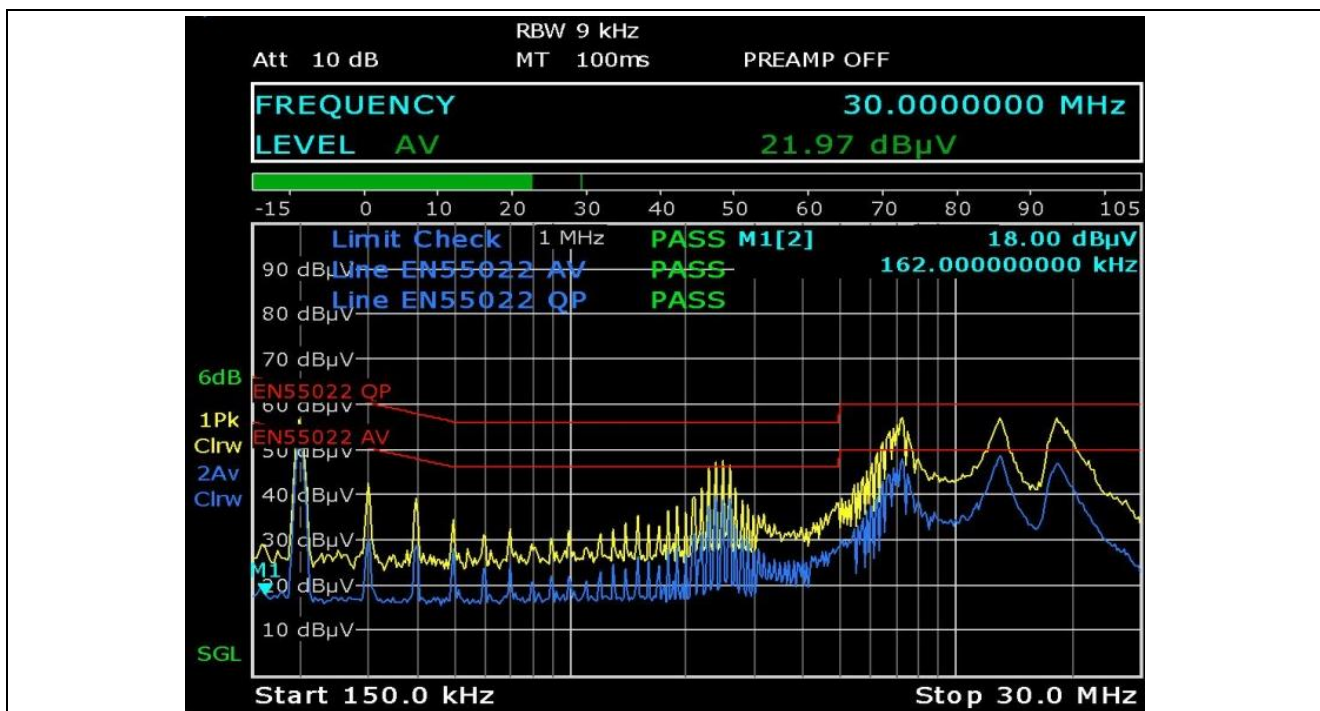


Figure 25 Conductive EMI measurement of the board with resistive load

5.3 Startup behavior

During power up when the V_{OUT} is less than 96% of the rated level, internal voltage loop output increases from initial voltage under the soft-start control. This results in a controlled linear increase of the input current from 0 A thus reducing the current stress in the power components as can be seen on the yellow waveform in Figure 26.

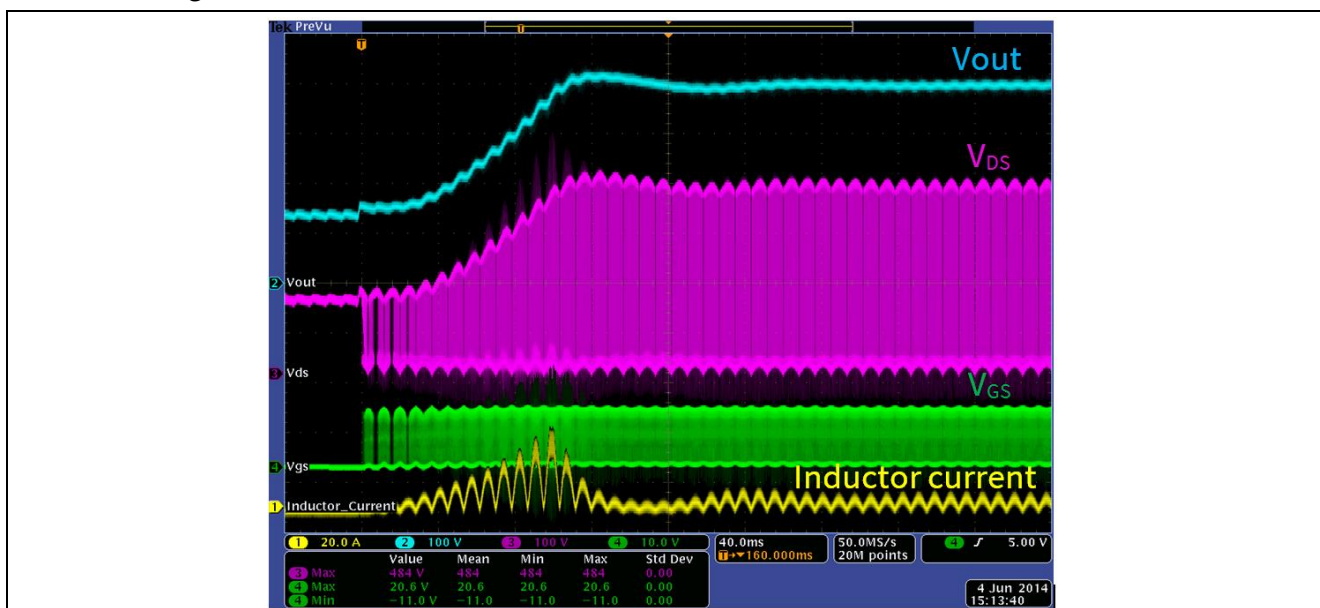


Figure 26 Waveform capture during low-line startup

6 Board design

6.1 Schematics

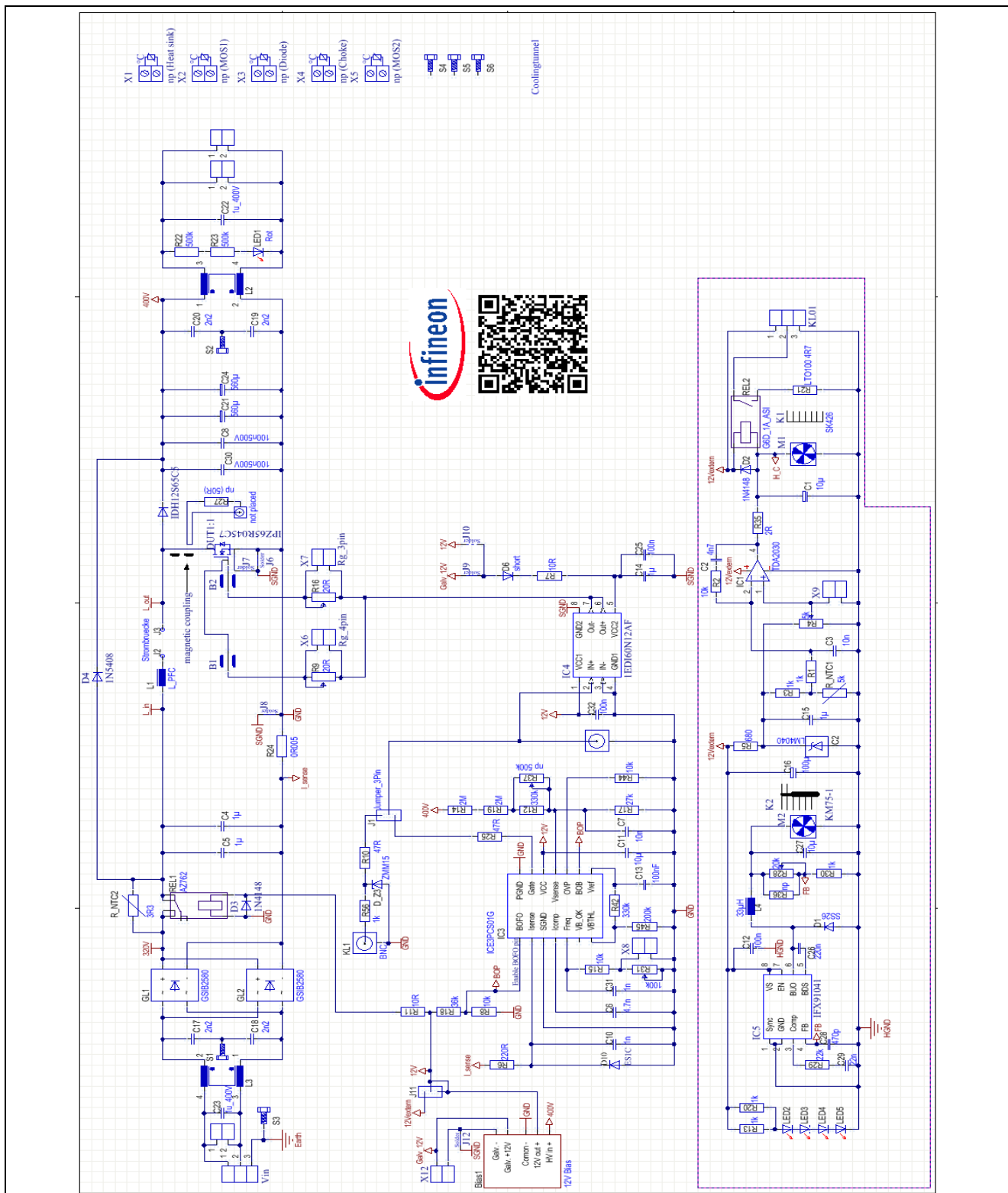


Figure 27 Evaluation board schematic

6.2 PCB layout

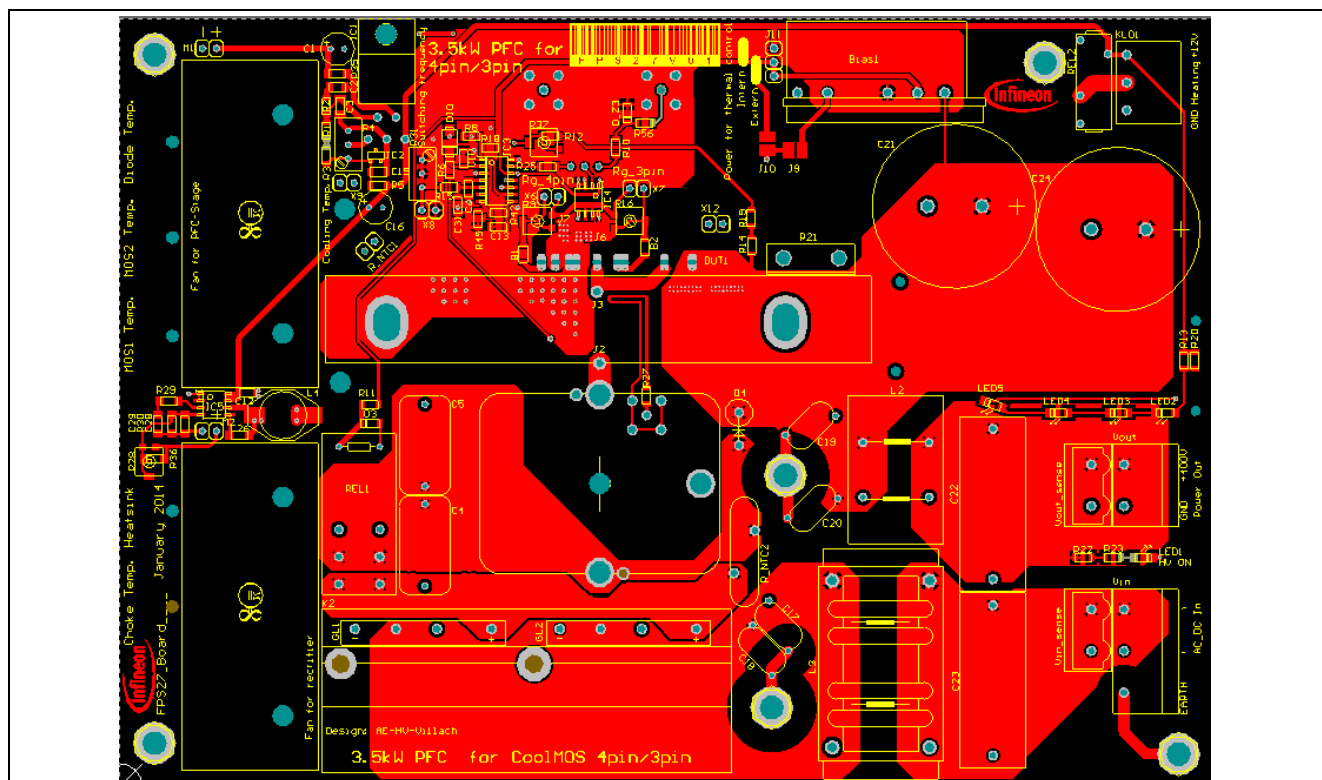


Figure 28 PCB top layer view

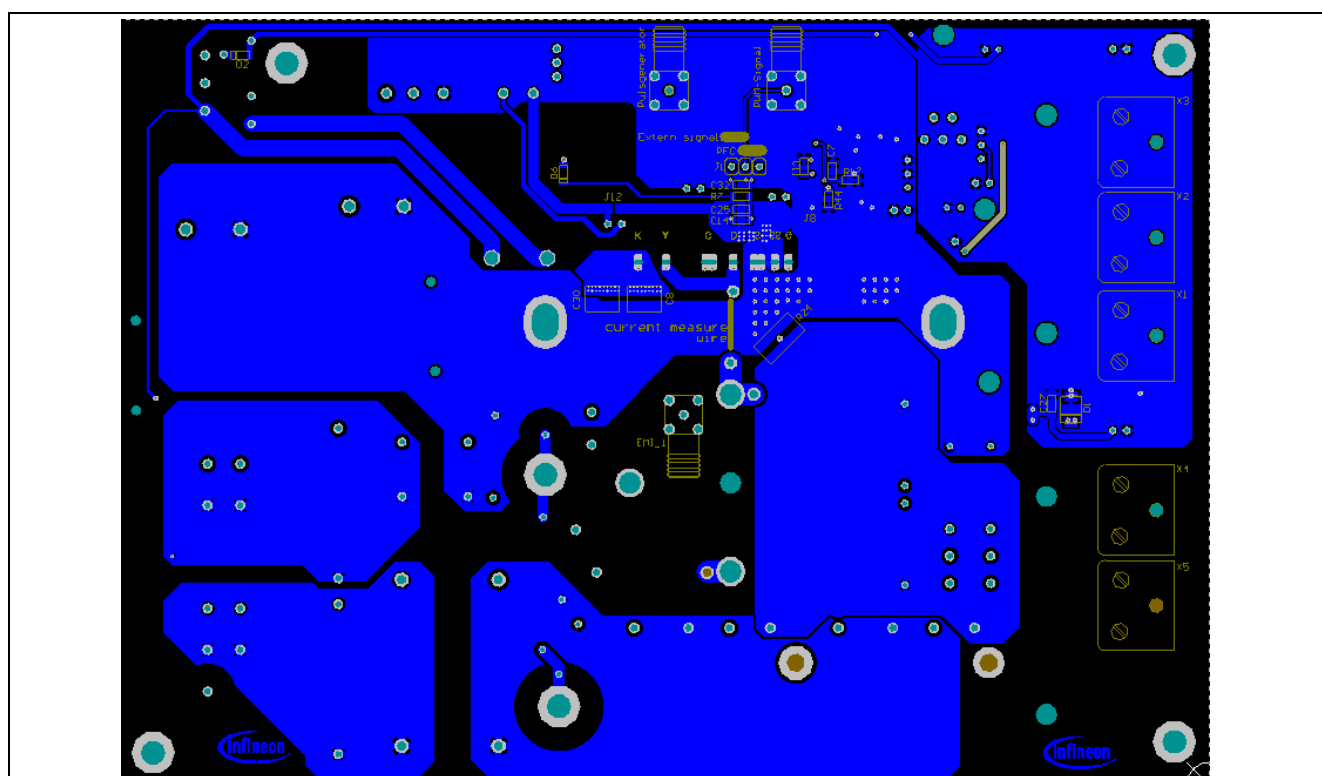


Figure 29 PCB bottom layer view

6.3 Bill of material

Table 3 Bill of material

Designator	Value	Description
B1, B2	closed with 0 Ω	Placeholder for Ferrite Bead, 0 Ω resistor
Bias1	12 V Bias	Bias adapter
C1	10 μ	25 V
C2	4n7	25 V
C3	10 n	25 V
C4, C5	1 μ	x-capacitor
C6	4.7 n	25 V
C7	10 n	25 V
C8, C30	100n500 V	VJ1825Y104KXEAT
C10, C31	1 n	25 V
C11	10 μ	25 V
C12, C25, C32	100 n	25 V
C13	100 n	25 V
C14, C15	1 μ	25 V
C16	100 μ	25 V
C17, C18	1.1 n	Y-capacitor
C19, C20	3.3 n	Y-capacitor
C21, C24	560 μ	EETHC2G561KA or EKMR421VSN561MR50S
C22	1u_400 V	BFC237351105; Farnel 1215540
C23	1.5u_400 V	
C26	220 n	25 V
C27	10 μ	25 V
C28	470p	25 V
C29	22n	25 V
D1	SS26	
D2, D3	1N4148	
D4	1N5408	
D6	short	0 Ω
D10	ES1C	1 A 150 V fast diode
DUT1	IPZ65R045C7	
D_Z3	ZMM15	1N4734A
EMI_1	not placed	EMI Adapter
GL1, GL2	GSIB2580	GSIB2580
IC1	TDA2030	Mount with M2.5x6
IC2	LM4040	LM4040D20IDBZRG4
IC3	ICE3PCS01G	PFC_CCM_Controller
IC4	1EDI60N12AF	6 A_isolated_MOSdriver
IC5	IFX91041	1.8A Step down switching regulator
J1, J11	Jumper_3Pin	SPC20486
J2	Current measure bridge	1.25 mm isolated copper wire
J3	Current measure bridge	U-shape-Cu-wire 1.25 mm 2 cm distance
J6	open	Solder jumper; 4 pin as 3 pin
J7, J12	close with solder	Solder jumper; driver ground to SS, Solder jumper; isolated driver power
J8, J10	open	Solder jumper; 3pin ground, Solder jumper; driver power none isolated
J9	close with solder	Solder jumper; isolated driver power
K1	SK426	100 mm long; mound with 2xM4x15
K2	KM75-1	KM75-1 +4clip 4597; Fischer
KL1	BNC	Oscilloscope_ Funtion generator
KL01	HV in	GMSTBVA 2,5 HC/ 3-G-7,62
KL01-S	Complement	GMSTB 2,5 HCV/ 3-ST-7,62
KL02	Vin_sense	GMSTBVA 2,5 HC/ 2-G-7,62
KL02-S	Complement	GMSTB 2,5 HCV/ 2-ST-7,62

L1	L_PFC	2times 77083A7 64wind_1.15 mm
L2	10 A 100 μ H	Würth 744824101
L3	8120-RC	BOURNS_8120-RC_2m4H_17 A
L4	33 μ H	74454133
LED1	red	Power on LED
LED2, LED3, LED4, LED5	blue	Power on LED
M1, M2	Fan 60mm	PMD1206PTB1-A
M1, M2	finger guard for Fan 60mm	LZ28CP
PWM-Signal	SMA	Oscilloscope_ Function generator
R1, R3, R13, R20, R56	1 k	5%
R2, R8, R15, R44	10 k	5%
R4	5 k	67WR20KLF
R5	680	5%
R6	220R	5%
R7, R11	10R	5%
R9, R16	20R	3314G-1-200E
R10, R25	47R	5%
R12, R42	330 k	5%
R14, R19	2M	5%
R17	27 k	5%
R18	36 k	5%
R21	LTO100 4R7	include two 20F2617 Bürklin connector
R22, R23	500 k	10%
R24	0R005	FCSL90R005FE
R27	np	
R28	20 k	23AR20KLFTR
R29	22 k	5%
R30	1 k	10 V
R31	100 k	67WR100KLF
R35	2R	5%
R36	np	
R37	np 500 k	5%
R45	200 k	5%
REL1	AZ762	12 V
REL2	G6D_1A_ASI	12 V
R_NTC1	5k	B57560G502F mound in K1 under MOS
R_NTC2	3R3	R_SL22
S1, S2, S3, S4, S5, S6	SCREW_M4	3 cm Distance holder
S1, S2, S3, S4, S5, S6	M4 Screw nut	M4 Screw nut
S1, S2, S3, S4, S5, S6	washer M4	washer M4
V _{in}	HV_in	GMSTBA_2.5HC_3G7.62
V _{out}	V _{out}	GMSTBA_2.5HC_2G7.62
V _{out_sense}	V _{out_sense}	GMSTBVA_2.5HC_2G7.62
X1	np (Heat sink)	thermocouple plug
X2	np (MOS1)	thermocouple plug
X3	np (Diode)	thermocouple plug
X4	np (Choke)	thermocouple plug
X5	np (MOS2)	thermocouple plug
X6	Rg_4pin	SPC20485
X7	Rg_3pin	SPC20485
X8, X9	KL_STANDARD_2	SPC20485
X12	Np	for adapter power supply

7 References

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8 Symbols used in formulas

Table 4 Symbols used in formulas

V_{ac}	Input voltage
$V_{ac,min}$	Minimum input voltage
V_o	Output voltage
P_o	Output power
f	Switching frequency
T	Switching time period
f_{line}	line frequency
L	Filter inductor
%Ripple	Inductor current ripple percentage to input current
DCR	Inductor DC resistance
$I_{in,rms}$	Input rms current
$I_{L,rms}$	Inductor rms current
$I_{L,avg}$	Inductor average current across the line cycle
$I_{L,pk}$	Inductor peak current
$P_{L,cond}$	Inductor conduction loss
$V_{f,bridge}$	Bridge diode forward voltage drop
P_{bridge}	Bridge power loss
$R_{on(100C)}$	MOSFET on-resistance at 100°C
Q_{gs}	MOSFET gate-source charge
Q_{gd}	MOSFET gate-drain charge
Q_g	MOSFET total gate charge
R_g	MOSFET gate resistance
V_{pl}	MOSFET gate plateau voltage
V_{th}	MOSFET gate threshold voltage
t_{on}	MOSFET turn-on time
t_{off}	MOSFET turn-off time
E_{oss}	MOSFET output capacitance switching energy
$I_{s,rms}$	MOSFET rms current over the line cycle
$P_{s,cond}$	MOSFET conduction loss
$P_{s,on}$	MOSFET turn-on power loss
$P_{s,off}$	MOSFET turn-off power loss
$P_{s,oss}$	MOSFET output capacitance switching loss
$P_{s,gate}$	MOSFET gate drive loss
$I_{D,avg}$	Boost diode average current
$V_{f,diode}$	Boost diode forward voltage drop
Q_{rr}	Boost diode reverse recovery charge

V_{ac}	Input voltage
P_{Dcond}	Boost diode conduction loss
$P_{D,sw}$	Boost diode switching loss
C_o	Output capacitor
ESR	Output capacitor resistance
t_{hold}	Hold-up time
$V_{o,mi}$	Hold up minimum output voltage
ΔV_o	Output voltage ripple
$I_{Co,rms}$	Output capacitor rms current
P_{Co}	Output capacitor conduction loss

Revision history

Major changes since the last revision

Page or reference	Description of change
--	First release (Revision 1.0)
Figure 8-12	Corrected output power on y-Axis: 10,000(Revision 1.1.)

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